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par

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Développement d'un capteur de nouvelle génération et son électronique intégrée pour les collisionneurs futurs

New Generation of Monolithic Active Pixel Sensors for Charged Particle Detection

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Wstęp

Projekt badań ukierunkowanych na rozwój nowej generacji detektorów pikselowych zintegrowanych z elektroniką odczytową został zainicjowany przez współpracujące grupy badawcze z francuskich laboratoriów Institut de Recherches Subatomiques (IReS) i Laboratoire d'Electronique et de Physique des Systèmes Instrumentaux (LEPSI) ze Strasbourga oraz partnera polskiego Katedry Elektroniki Akademii Górniczo Hutniczej w Krakowie. Prace badawcze związane z przygotowywaną rozprawą doktorską prowadzone były w ramach porozumienia "thèse en co-tutelle" zawartego między Akademią Górniczo-Hutniczą w Krakowie i Uniwersytetem L. Pasteura w Strasbourgu. Celem pracy były badania związane z projektem nowej generacji półprzewodnikowego detektora promieniowania jonizującego, który pozwoliłby na integrację na tym samym podłożu elementów czułych na promieniowanie oraz stowarzyszonej elektroniki rejestrująco-odczytowej. Prowadzone prace badawcze ukierunkowane były zasadniczo na zastosowania w eksperymentach fizyki wysokich energii, do detekcji i określania torów wysokoenergetycznych cząstek jonizujących w konstrukcji detektora wierzchołka na potrzeby eksperymentów fizyki wysokich energii w planowanych do budowy akceleratorach liniowych. Możliwe są również aplikacje w innych dziedzinach, takich jak obrazowanie w zastosowaniach medycznych lub w eksperymentach prowadzonych w przestrzeni kosmicznej, dozymetrii, do prowadzenia monitorowania intensywności wiązek promieniowania, itp. Zastosowania te mogą być związane z detekcją promieniowania X, β oraz α w szerokim zakresie energii.

Rosnące wymagania nałożone na parametry detektorów wierzchołka w planowanych eksperymentach fizyki cząstek elementarnych, prowadzonych przy wykorzystaniu urządzeń, w których dochodzi do zderzeń elektronów i pozytronów z dwóch naprzeciw bieżnych (*ang. linear collider*) wiązek o wysokich intensywnościach (*ang. luminosity*) oraz przyspieszanych do wysokich energii w zakresie TeV, wiążą się z koniecznością użycia nowych, monolitycznych o zmniejszonej ilości materiału na drodze przelatujących cząstek, o dużej szybkości działania i o wysokiej rozdzielczości przestrzennej oraz o niskim poborze mocy detektorów półprzewodnikowych. Niekomercyjne zastosowanie urządzeń wymusza również niski koszt

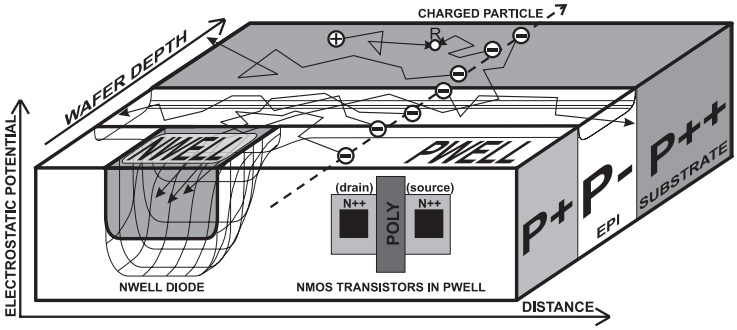
fabrykacji układów, a konieczność zapewnienia poprawnej i długotrwałej, bez utraty pierwotnych parametrów, pracy w środowisku o wysokim tle radiacyjnym kładzie nacisk na dużą odporność na efekty związane z dużymi dawkami napromieniowania. Ponadto preferowane są rozwiązania pozwalające na implementację realizowanych funkcji w postaci gotowych "inteligentnych" systemów scalonych *(ang. system-on-chip)*. Wymagania te zmniejszają znacząco atrakcyjność dotychczas stosowanych rozwiązań, takich jak układy o sprzężeniu ładunkowych *(ang. Charge-Coupled Devices - CCD)* lub pikselowych detektorów hybrydowych *(ang. Hybrid Pixel Detectors - HPD)*. Proponowane w tej pracy monolityczne detektory typu aktywne piksele *(ang. Monolithic Active Pixel Sensors - MAPS)* realizowane przy wykorzystaniu standardowego procesu CMOS są w stanie spełnić wymienione wyżej wymagania do detekcji i określania torów cząstek minimalno-jonizujących. Praca ta ukazuje szczegóły projektowe detektorów MAPS mające związek z procesem ich fabrykacji. Przedstawiona jest również dyskusja rezultatów otrzymanych przy wykorzystaniu fabrykowanych struktur prototypowych, wystawionych na działanie źródeł radioaktywnych i wysokoenergetycznych wiązek cząstek jonizujących. Prezentacja wyników testów jest poprzedzona analizą teoretyczną układów elektronicznych, z uwzględnieniem analizy szumowej, i symulacją działania detektora na poziomie fizycznym.

Detektory pikselowe CMOS pojawiły się na przestrzeni ostatniej dekady, jako konkurencyjne rozwiązanie dla układów CCD w komercyjnych zastosowaniach do detekcji światła widzialnego *(ang. on-chip camera)*. Obecnie obserwowana jest silna ekspansja wizyjnych układów CMOS w cyfrowych aparatach fotograficznych i kamerach video. Bezpośrednie użycie urządzeń komercyjnych do zastosowań wymagających detekcji cząstek jonizujących jest niemożliwe. Układy tego typu często wykorzystują konstrukcję elementu aktywnego nie zapewniającą pełnego pokrycia powierzchni detektora *(ang. fill factor)* oraz ich architektury nie przystają konceptualnie do specyfikacji narzuconych przez konstrukcje systemów detektorowych w eksperymentach fizycznych.

Zasada działania

Wydajne zbieranie ładunku generowanego przez przelatujące przez detektor cząstki, może zostać osiągnięte przy użyciu warstwy epitaksjalnej o niskim poziomie domieszkowania jako aktywnej części detektora. Warstwa epitaksjalna, wytwarzana w procesie wzrostu na podłożu o zazwyczaj wysokim poziomie domieszkowania typu P, jest dostępna w licznych

procesach technologicznych CMOS używanych do fabrykacji scalonych układów wielkiej skali integracji. Dokładny obraz proponowanej struktury jest przedstawiony na rysunku 1, który ukazuje przekrój przez warstwowy układ wafla *(ang. wafer)* używanego do fabrykacji wraz z zaznaczeniem rozkładu potencjału elektrycznego wewnątrz struktury. Struktura detektora składa się z dwóch elementów: pierwszym z nich jest głęboka studnia o typie domieszkowania N, która tworzy wraz z podłożem epitaksjalnym złącze pn (dioda nwell/p-epi) i pełni rolę elementu zbierającego ładunek, drugim elementem jest studnia o typie domieszkowania P, która jest używana jako podłoże dla układu elektroniki odczytowej umiejscowionej w każdym pikselu.

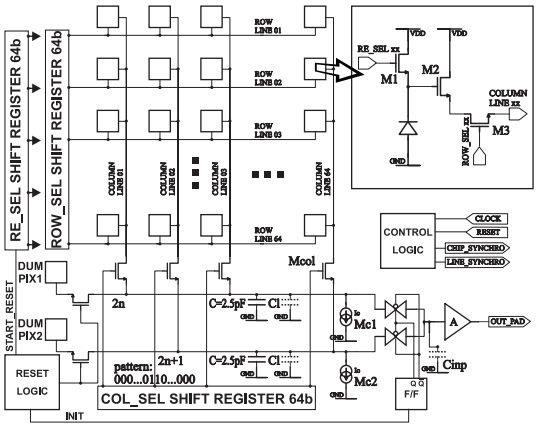


Rysunek 1. Przekrój przez strukturę detektora MAPS dla detekcji i określania torów cząstek jonizujących

Obydwie studnie są implantowane w warstwie epitaksjalnej, która podobnie jak podłoże posiada typ domieszkowania P. W związku z różnymi poziomami domieszkowania obecne są bariery potencjału pomiędzy warstwą epitaksjalną a studnią typu P i podłożem. Obecność barier potencjału utrzymuje wolne elektrony, wytworzone w procesie jonizacji, w obrębie warstwy epitaksjalnej. Nośniki te poruszają się dzięki procesowi dyfuzji termicznej i są w następstwie ruchu zbierane przez diody nwell/p-epi. W wyniku procesu zbierania ładunku generowany jest sygnał elektryczny na pikselach znajdujących się w pobliżu miejsca przelotu cząstki. Ładunek uwalniany w podłożu jako wynik procesu jonizacji jest w większości tracony z powodu szybkiej rekombinacji nośników związanej z wysokim poziomem domieszkowania w tej części ośrodka. Ilość dostępnego ładunku generującego sygnał jest proporcjonalna do grubości warstwy epitaksjalnej.

Pojedyncza komórka piksela zawiera w swojej podstawowej strukturze wcześniej opisaną diodę oraz trzy tranzystory NMOS. Na obszarze matrycy aktywnych pikseli projekt układu elektronicznego jest ograniczony wyłącznie do tranzystorów NMOS. Natomiast na częściach

zewnętrznych detektora obydwa komplementarne typy tranzystorów mogą być używane. Prototypowe układy detektorowe zostały wyposażone w sekwencyjny odczyt sygnału analogowego niosącego informację o aktualnym poziomie napięć na poszczególnych pikselach w testowanej matrycy. Rysunek 2 przedstawia uproszczony schemat jednego z prototypów. W oknie powiększenia pokazana jest struktura piksela, w której tranzystor M1 pełni rolę klucza umożliwiającego uzyskanie wstecznej polaryzacji diody *(ang. reset transistor)*, tranzystor M2 wraz z połączeniem ze źródłem prądu realizowanym przy wykorzystaniu tranzystora NMOS stanowi wtórnik źródłowy. Prąd ze źródła jest przełączany do zaadresowanych pikseli a źródło prądu zostało zaprojektowane jako wspólne dla wszystkich kolumn w matrycy pikseli. Adresowanie poszczególnych pikseli do odczytu zachodzi przy użyciu kluczy tranzystorowych M3 i Mcol. Dominującym źródłem szumów w układzie jest szum kTC związany z sekwencyjnym zamykaniem i otwieraniem klucza M1. W celu eliminacji tego przyczynku szumowego technika bazująca na korelacji czasowej próbkowanego sygnału *(ang. Correlated Double Sampling – CDS)* była używana do przetwarzania sygnału. Obróbka danych była przeprowadzana programowo na wartościach numerycznych sygnałów zapisywanych do pliku dyskowego w procesie zbierania danych.



Rysunek 2. Uproszczony schemat układu MIMOSA II

Wykonana praca

Wydajna detekcja cząstek minimalno jonizujących została zademonstrowana dla pierwszego prototypu zaprojektowanego i wykonanengo w ramach przyjętego planu pracy. Prototypowy układ MIMOSA I* został zrealizowany w procesie CMOS AMS 0.6 μm,

* MIMOSA signifie en anglais Minimum Ionising MOS Active pixel sensor.

a następnie poddany testom laboratoryjnym oraz przy wykorzystaniu wiązki wysokoenergetycznych cząstek w CERN*. Układ zawierał cztery niezależne matryce o wymiarach 64 × 64 piksele. Wymiar matrycy został wybrany jako kompromis między minimalnym rozmiarem, przy którym możliwe jest przeprowadzenie wydajnych testów, a kosztem fabrykacji. Testy przeprowadzone dla układu MIMOSA I potwierdziły wydajność detekcji cząstek minimalno-jonizujących, dla wymiarów piksela (długość × szerokość × grubość warstwy epitaksjalnej) = 20 μm × 20 μm × 15 μm.

Symulacje działania detektora zostały przeprowadzone przy użyciu komercyjnego pakietu symulacyjnego ISE–TCAD przeznaczonego do symulacji na poziomie fizycznym działania elementów półprzewodnikowych i ich procesu fabrykacji. Symulacje detektorów MAPS były przeprowadzone przy użyciu modelu trójwymiarowego. Otrzymane wyniki pozwoliły na estymację wielkości zbieranego ładunku dla struktury odpowiadającej topologii układu MIMOSA I na poziomie pomiędzy 800 a 1000 elektronów dla przypadku pojedynczej cząstki przelatującej przez detektor oraz czasu zbierania ładunku na poziomie 100 ns. W celu estymacji ilości zbieranego ładunku zostały poczynione odpowiednie założenia na parametry używanego procesu i topologii symulowanego układu. Jako parametry symulacji zostały użyte takie wielkości, jak: liczba diod połączonych równolegle w obrębie jednego piksela, ich wzajemny rozkład, wymiary geometryczne diody, wymiary piksela oraz grubość warstwy epitaksjalnej.

Bezwzględna wartość wzmocnienia układu detekcyjnego została wyznaczona dla fabrykowanych prototypów w wyniku przeprowadzenia ich kalibracji. Do tego celu zostały wykorzystane dwie niezależne metody pomiarowe: pomiary wykonane przy użyciu źródła niskoenergetycznych fotonów promieniowania X pochodzącego ze źródła ^{55}Fe (5.9 keV) oraz analizy wykorzystującej zależność statystyczną, zgodną z rozkładem Poissona, pomiędzy mierzonym szumem śrutowym i wartością średnią sygnału. Wartość mierzonego współczynnika wzmocnienia wyraża zależność między mierzonym sygnałem napięciowym a zebranym ładunkiem na pojemności detektora.

Zmierzone parametry, odwołujące się do detekcji relatywistycznych cząstek minimalno-jonizujących, obejmują wydajność detekcji na poziomie powyżej 99% oraz osiągniętą

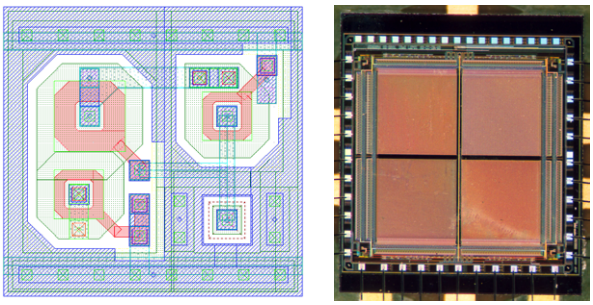
* CERN - European Organisation for Nuclear Research.

rozdzielczość przestrzenną około 1.4 μm. Zmierzona charakterystyka szumowa, która nie została w pełni zoptymalizowana w pierwszym prototypie, była w pełni zgodna z symulacjami przeprowadzonymi przy użyciu programu SPICE. W wyniku pomiarów otrzymano wielkość zastępczego ładunku szumów przeniesionego na wejście piksela *(ang. Equivalent Noise Charge – ENC)* na poziomie pomiędzy 14 e^- a 30 e^-. Tak niski poziom szumu pociągał korzystną wartość stosunku sygnału do szumu *(ang. Signal-to-Noise Ratio – SNR)* na poziomie 30 do 40, która to wartość pozwoliła na lokalizację przelatujących cząstek z rozdzielczością znacznie lepszą niż wymiary piksela.

Jako kontynuacja prac nad układem MIMOSA I zostały zaprojektowane cztery inne prototypy i wykonane przy użyciu procesów 0.25 μm, 0.35 μm z warstwą i bez warstwy epitaksjalnej oraz 0.6 μm. Struktura nowych układów została poddana optymalizacji, która dotyczyła zwiększenia prędkości odczytu (40 – 50 MHz częstotliwość zegara odczytowego) oraz minimalizacji szumu. Najlepsza zmierzona wartość szumu, liczonego jako wariancja sygnału próbkowanego po zastosowaniu przetwarzania za pomocą filtracji CDS, kształtowała się na poziomie 8 e^- i wartość ta została osiągnięta dla częstotliwości zegara odczytowego 10 MHz dla układu MIMOSA III. W kolejnych układach testowane były nowe struktury elementów czułych na promieniowanie, takie jak: photoFET lub struktura piksela, w którym wyeliminowano tranzystor resetu, zastępując jego działanie automatyczną wsteczną polaryzacją diody zbierającej ładunek. Testowane były również specjalne struktury mające na celu przeprowadzenie wiarygodnych testów odporności na dawki promieniowania jonizującego i neutronów. Końcowym etapem badań, stanowiących przedmiot zainteresowania w tej pracy, była fabrykacja detektora w postaci pojedynczego układu scalonego o wymiarach 19400 × 17350 μm^2 zawierającego w swojej strukturze 10^6 pikseli. Układ ten, posiadający wymiary praktycznego detektora, przewidziany jest jako podstawowy element "listewki" zawierającej kilka układów tego typu i mogącej znaleźć zastosowanie w praktycznych aplikacjach.

Schemat blokowy projektowanych prototypów na przykładzie układu MIMOSA II pokazany jest na rysunku 2. Projekt tego detektora wykorzystuje odczyt sygnału analogowego z naprzemienną multipleksacją na wzmacniacz wyjściowy kolumn parzystych i nieparzystych. W systemie takim możliwe jest polepszenie charakterystyki szumowej przez znaczące zmniejszenie pasma częstotliwościowego wtórników źródłowych przy jednoczesnym

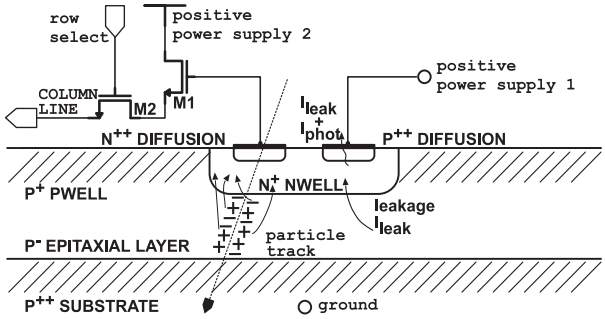
zachowaniu dużej szybkości odczytu. Cel ten osiągnięto dzięki przygotowywaniu piksela z kolumny będącej następną w kolejce do odczytu w chwili odczytywania piksela z kolumny bieżącej.



Rysunek 3. Projekt layoutu piksela z tranzystorami posiadającymi bramki w postaci zamkniętej dla układu MIMOSA III (na lewo), mikrofotografia prototypu MIMOSA IV (na prawo)

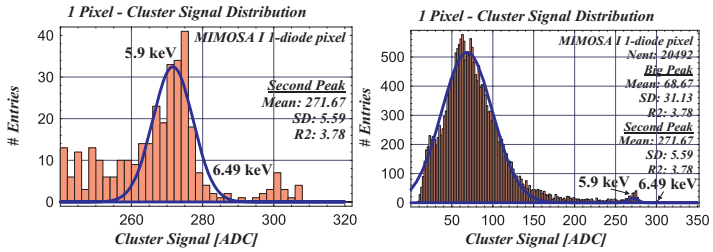
Kompletny projekt layoutu matrycy aktywnych pikseli wraz z układem elektroniki odczytowej prototypu MIMOSA III został wykonany z wykorzystaniem reguł layoutowych pozwalających na osiągnięcie dużej odporności układów scalonych realizowanych w procesach sub-mikronowych na dawki promieniowania jonizującego. Reguły te polegają na użyciu tranzystorów NMOS posiadających bramki w postaci zamkniętych pierścieni oraz na konsekwentnym stosowaniu pierścieni ochronnych *(ang. guard-rings)* wokół każdego obszaru o domieszkowaniu typu N. Głównym celem fabrykacji układu MIMOSA III było przeprowadzenie niezbędnych pomiarów pozwalających na oszacowanie granic odporności nowej technologii na zniszczenia radiacyjne. Wstępne wyniki testów wskazują na odporność detektorów MAPS na promieniowanie zarówno w zakresie do kilkuset krad dawki promieniowania jonizującego, jak i około 10^{12} n/cm^2 całkowitego zintegrowanego strumienia dawki ekwiwalentnej 1 MeV neutronów. Rysunek 3 pokazuje przykład projektu pojedynczego piksela o wymiarach 8×8 μm^2 zaprojektowanego według opisanych wyżej reguł. Rysunek ten pokazuje również mikrofotografię kolejnego prototypu MIMOSA IV, którego projekt zawiera testowe struktury nowych rozwiązań elementów detekcyjnych. Badania nowych struktur elementów aktywnych ukierunkowane były na implementację wzmocnienia sygnału bezpośrednio w strukturę elementu zbierającego ładunek, na zastąpienie okresowego resetowania piksela przez automatyczną wsteczną polaryzację diody oraz na umożliwienie bezpośredniego odczytu sygnału różnicowego przez implementację ekwiwalentu CDS bezpośrednio na poziomie piksela. Jednym z takich udoskonaleń jest dwudiodowa struktura

piksela o logarytmicznej charakterystyce odpowiedzi napięciowej pokazana na rysunku 4. Innym proponowanym rozwiązaniem jest element aktywny o odpowiedzi w trybie prądowym wykorzystujący efekt wzmocnienia w obrębie elementu aktywnego o przyjętej nazwie photFET. Oba rozwiązania pozwalają na automatyczną wsteczną polaryzacje diody zbierającej ładunek.



Rysunek 4. Zasada działania piksela o automatycznej wstecznej polaryzacji diody nwell/p-epi.

Rysunek 5 pokazuje przykładowe wyniki, osiągnięte w spektroskopii fotonów promieniowania X o energii 5.9 keV, pozwalające na estymację wartości wzmocnienia konwersji ładunku na napięcie na przykładzie układu MIMOSA I.

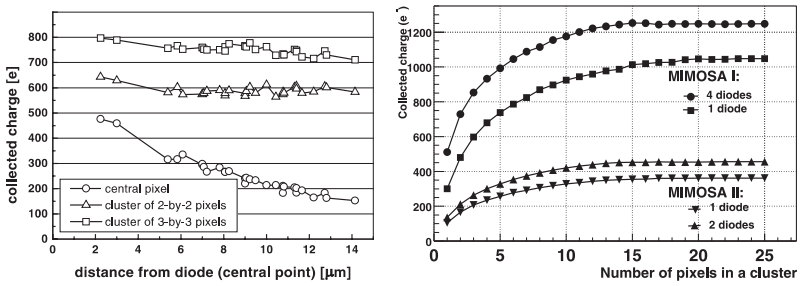


Rysunek 5. Kalibracja bezwzględnej wartości wzmocnienia konwersji ładunku na napięcia w przypadku układu MIMOSA I przy wykorzystaniu fotonów promieniowania X o energii 5.9 keV.

Drugi, o znacznie mniejszej liczbie wejść „pik", obecny na histogramach, odpowiada konwersji fotonów w obszarze warstwy zubożonej diody nwell/p-epi i reprezentuje 100% wydajność zbierania ładunku. Interpretacja obecności drugiego „piku" w spektrum fotonów pozwoliła na opracowanie metody kalibracji, w której położenie tego „piku" brane jest do wyznaczania dokładnej wartości wzmocnienia.

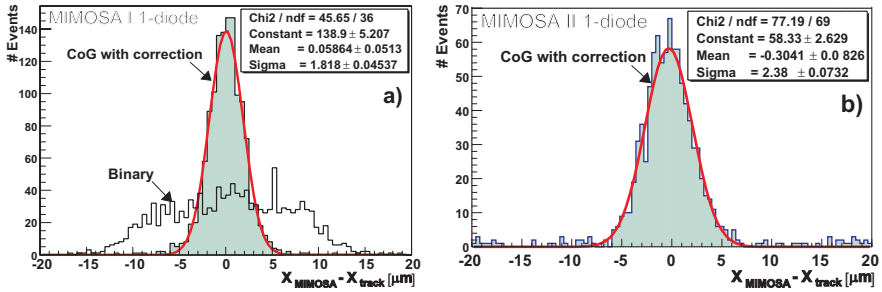
Wydajność oraz czas zbierania ładunku generowanego przez cząstki minimalno-

jonizujące były poddane intensywnym symulacjom przy wykorzystaniu pakietu ISE-TCAD. Rysunek 6 pokazuje przykładowe wyniki symulacji zestawione w celu porównania z otrzymaną eksperymentalnie zależnością liczby zebranych elektronów w funkcji liczby pikseli, z których sumowano sygnały *(ang. cluster)*.



Rysunek 6. Wydajność zbierania ładunku – przykład wyników uzyskanych w symulacjach przy użyciu pakietu ISE-TCAD (wykres lewy), rozkład liczby zbieranych elektronów otrzymany w wyniku przeprowadzonych testów na wiązce wysokoenergetycznych cząstek (wykres prawy).

Rysunek 7 przedstawia wyniki pomiarów rozdzielczości przestrzennej zmierzonej dla detektorów MAPS na przykładzie układów MIMOSA I i II.



Rysunek 7. Rozkład rezydualny położenia mierzonego toru cząstki przez matrycę pikseli o architekturze z pojedynczą diodą zbierającą ładunek w przypadku prototypu MIMOSA I, przy użyciu dwóch algorytmów analizy danych: dla metody pozwalającej na oszacowanie binarnej rozdzielczości przestrzennej i dla wyliczenia środka ciężkości zbieranego ładunku z poprawką nieliniową (wykres lewy), odpowiedni rozkład dla układu MIMOSA II (wykres prawy).

Otrzymane wielkości z dużym marginesem bezpieczeństwa spełniają wymagania stawiane detektorowi wierzchołka przeiwidzianemu na potrzeby przyszłych eksperymentów zderzeniowych planowanych na nowobudowanych akceleratorach liniowych.

Podsumowanie

W pracy tej została zaproponowana i rozwinięta idea monolitycznego detektora

pikselowego, wykorzystującego jako element bazowy klasyczną strukturę opartą o układ składający się z trzech tranzystorów w obrębie każdej komórki matrycy. Zastosowania tego typu detektorów mogą być znacznie szersze niż aplikacje z zakresu fizyki wysokich energii do detekcji i określania torów cząstek minimalno-jonizujących. Mogą one obejmować szeroki zakres obrazowania wykorzystującego promieniowanie jonizujące. Konkretne aplikacje będą wymagały optymalizacji układowej elektroniki odczytowej oraz samego elementu aktywnego.

Należy podkreślić główną zaletę monolitycznych detektorów pikselowych realizowanych przy wykorzystaniu standardowych procesów fabrykacji układów scalonych CMOS w postaci ich szerokiego i zróżnicowanego pola zastosowań. Aspekt interdyscyplinarny zastosowań tego typu urządzeń oraz silna presja komercyjna ukierunkowana na aplikacje mające zastosowanie do światła widzialnego są gwarantem kontynuacji rozwoju technologicznego. Związane jest to ze stałym dostępem do nowych procesów fabrykacji lepiej dostosowanych do stawianych wymagań (wliczając minimalizację prądów upływu, powiększenie gęstości upakowania, zwiększenie odporności na promieniowanie itp.) oraz pozwalających na osiągnięcie dużej elastyczności w prowadzeniu projektów. Nowoczesne technologie fabrykacji układów scalonych pozwalają na integrację detektora wraz z elektroniką odczytową na wspólnym podłożu. Rozwój na skalę laboratoryjną procesu dedykowanego do fabrykacji specjalizowanych układów, jakimi są tego typu detektory, wiąże się z wysokimi kosztami i nie gwarantuje stabilności a przez to odpowiedniego uzysku procesu. W przeciwieństwie do tego użycie standardowych procesów komercyjnych pozwala na wysoki uzysk, co w konsekwencji prowadzi do gwarancji sukcesu projektu. Środowisko fizyki eksperymentalnej wysokich energii może w ten sposób korzystać z szybkiego rozwoju technologii przemysłowych do budowy systemów detekcyjnych o wysokiej rozdzielczości.

RESUMÉ

Introduction

Le projet de développement d'un capteur de nouvelle génération et de son électronique intégrée pour les futurs collisionneurs, initié par les laboratoires IReS et LEPSI, a été mené dans le cadre d'une convention pour une thèse en co-tutelle entre l'Université Louis Pasteur de Strasbourg et l'Académie des Mines et de la Métallurgie de Cracovie en Pologne. Le but du travail était la conception d'un capteur de rayonnement ionisant de nouvelle génération qui pourrait intégrer sur le même substrat les éléments sensibles aux rayonnements et leur électronique de lecture. Le développement a été orienté vers les expériences de la physique de haute énergie et vers d'autres applications comme l'imagerie médicale, le spatial, etc. (détection des rayons X, beta, alpha etc.). Les développements récents de la physique des particules (collisionneurs linéaires de haute luminosité au TeV) conduisent à une demande accrue de nouveaux capteurs, intégrés, rapides, à haute résolution spatiale, à faible consommation de puissance, et intégrant des fonctions de plus en plus "intelligentes". La nécessité d'une production à faible coût et d'un fonctionnement satisfaisant en milieu hostile à cause des radiations, réduisent fortement l'attrait des capteurs CCD, et font des capteurs CMOS* à pixels de bons candidats à même de satisfaire l'ensemble de ces exigences.

Les capteurs CMOS sont apparus récemment dans le monde des applications commerciales comme les grands compétiteurs des CCDs† communément utilisés dans la détection des rayonnements lumineux (la photographie numérique et les applications vidéo). Ceci ne se restreint pas à la détection des photons visibles. Cette thèse présente les détecteurs monolithiques à pixels actifs (Monolithic Active Pixels Sensors – MAPS) réalisés en technologie CMOS standard pour la détection et la trajectographie de particules chargées faiblement ionisantes.

Les détails de la conception de ce nouveau type de capteur liés aux processus de leur fabrication sont présentés. La thèse discute aussi des résultats obtenus pendant les tests avec des sources radioactives et en faisceaux de particules de hautes énergies. Les résultats des

* CMOS – Complementary Metal Oxide Semiconductor

† CCDs - Charge-Coupled Devices

mesures sont précédés par une analyse théorique du réseau électrique (y compris l'analyse de bruit) et par des simulations physiques du fonctionnement du détecteur.

Principe de fonctionnement

La collection efficace de la charge libérée par une particule traversant le détecteur peut être atteinte en utilisant, comme volume actif, la couche faiblement dopée résultant d'un processus d'épitaxie. La couche épitaxiale que l'on fait croître sur le substrat de type P, habituellement fortement dopé, est disponible dans de nombreux processus de fabrication des circuits intégrés CMOS. La structure de détection proposée, est présentée en coupe dans la figure 1.

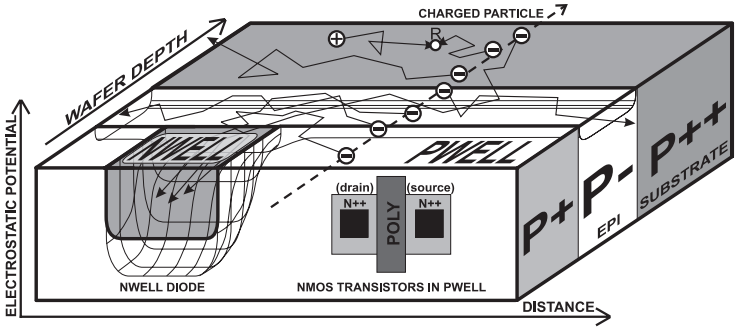


Figure 1. Coupe de la structure MAPS pour la détection et la trajectographie de particules chargées.

Elle se compose de deux éléments: un puits profond de type N qui joue le rôle d'élément collecteur de la charge, c'est une diode n-well/p-epi; un puits de type P utilisé comme substrat pour l'électronique de lecture de chaque pixel. Les deux puits sont implantés dans la couche épitaxiale qui est du type P, comme le substrat. Des barrières de potentiel réflectives pour les électrons existent entre le puits P et le substrat fortement dopé. Les électrons libérés dans le processus d'ionisation sont confinés dans la couche épitaxiale et diffusent vers les diodes n-well/p-epi où ils sont collectés. Ils génèrent un signal électrique sur le pixel proche du point de passage d'une particule. La charge libérée dans le substrat est, en majeur partie, perdue suite à la recombinaison rapide due au dopage élevé. La quantité totale de charge contribuant au signal est proportionnelle à l'épaisseur de la couche épitaxiale.

Le pixel individuel comprend la diode décrite ci-dessus et trois transistors de type N. Par contre, à la périphérie du capteur les deux types complémentaires de transistors sont utilisés. Les puces sont équipées d'un mode de lecture analogique en série. Dans la figure 2, le transistor M1 est utilisé pour rétablir la polarisation en inverse sur la diode, le transistor M2

constitue une moitié du suiveur avec une source de courant commune pour toutes les colonnes. Le transistor M3 et les transistors Mcols sont utilisés pour l'adressage des pixels. Le double échantillonnage corrélé (Correlated Double Sampling - CDS), effectué en différé sur les données acquises après numérisation, est utilisé pour éliminer le bruit kTC – la source dominante dans le bruit du système.

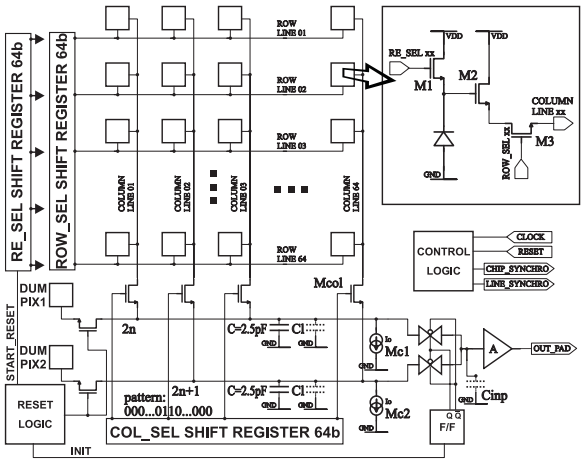


Figure 2. Synoptique de MIMOSA II.

Travail effectué

La détection de particules faiblement ionisantes a été démontrée sur un premier prototype réalisé dans le cadre du plan du travail. Le prototype MIMOSA I* a été réalisé en technologie CMOS AMS 0.6 μm, puis testé au laboratoire et en faisceau de particules de haute énergie au CERN†. Il comporte 4 matrices indépendantes de 64 par 64 pixels. C'est un compromis entre le coût et la taille minimale nécessaire pour un test en faisceau de particules. Cette étude a validé l'efficacité de détection, pour des particules faiblement ionisantes, d'un capteur à pixels de 20 μm et de 15 μm de couche épitaxiale. Le logiciel commercial, ISE-TCAD, de simulation physique des composants à la base de matériels semi-conducteurs a été utilisé. Les simulations du détecteur en utilisant un modèle en 3D donne 800 à 1000 électrons pour une particule traversant le détecteur. Pour calculer la quantité d'électrons collectés, des hypothèses ont été faites sur les paramètres de la technologie utilisée pour la fabrication du prototype en tenant compte de sa topologie. Celle-ci comprend le nombre de diodes connectées en parallèle, leur arrangement dans un pixel, la taille de la diode et la taille du

* MIMOSA signifie en anglais Minimum Ionising MOS Active pixel sensor

† CERN - European Organisation for Nuclear Research

pixel. Un calibrage absolu a été fait pour déterminer le gain du système de détection. Ceci a été possible en combinant les résultats des simulations avec les mesures de photons X de faible énergie provenant d'une source radioactive ^{55}Fe (5.9 keV). Le gain est exprimé en nombre d'électrons correspondant à la tension mesurée. La détection de particules relativistes, au minimum d'ionisation, s'est faite avec une efficacité supérieure à 99% et avec une résolution spatiale de l'ordre de 1.4 μm. Les performances de bruit, non optimisées dans ce premier prototype, sont conformes à la simulation SPICE et donnent entre 14 e^- et 30 e^- de bruit équivalent ramené à l'entrée. On obtient un rapport signal/bruit de l'ordre de 30 à 40 qui permet la détection individuelle et la localisation des particules avec une résolution meilleure que la taille des pixels. Suite à MIMOSA I, quatre autres prototypes ont été fabriqués respectivement en technologies 0.25 μm, 0.35 μm avec et sans couche épitaxiale et 0.6 μm. Ces nouveaux circuits ont été optimisés pour augmenter la vitesse de lecture jusqu'à 40 MHz – 50 MHz et pour diminuer le bruit. La meilleure valeur de bruit, mesurée et calculée comme la variance de signal échantillonné, s'approche de 8 e^- pour une fréquence de lecture de 10 MHz. Par la suite, des nouveaux éléments sensibles comme le photoFET, le pixel avec la mise à zéro automatique et des structures spéciales de test à la résistance aux rayonnements ionisants et aux particules lourdes ont été implantés. Un prototype à échelle réelle d'une taille de 19400 × 17350 μm^2 et comportant 10^6 pixels, a été mis en fabrication. C'est un élément de base d'une barrette de plusieurs circuits pour répondre aux applications. Le schéma synoptique du prototype MIMOSA II est présenté dans la figure 2. Dans ce circuit, la lecture analogique alternée de colonnes avec deux lignes de lecture multiplexées vers un amplificateur de sortie a été conçue.

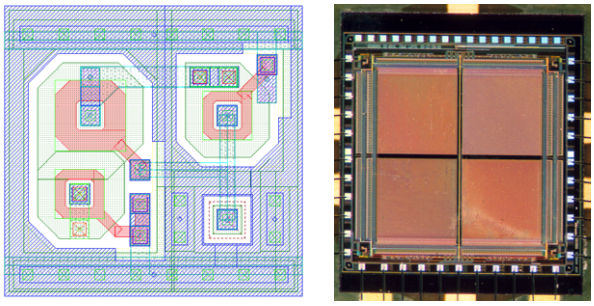


Figure 3. Dessin de masque d'un pixel avec les transistors possédant les grilles fermées dans MIMOSA III (à gauche) la micro-photographie du prototype (MIMOSA IV) (à droite).

Ceci permet l'augmentation de la vitesse de lecture et optimise le bruit. Le dessin de masques

d'un pixel avec des transistors à grilles fermées a été introduit dans le circuit MIMOSA III pour étudier et tester les limites de la résistance aux radiations. La figure 3 montre un exemple d'un pixel de la taille de $8 \times 8\ \mu m^2$ conçu selon les règles de l'électronique submicronique résistante aux radiations. Cette figure présente aussi la micro-photographie du prototype MIMOSA IV sur lequel les nouveaux éléments sensibles pour la détection ont été intégrés. La structure avec mise à zéro automatique, fait l'objet d'un dépôt de brevet.

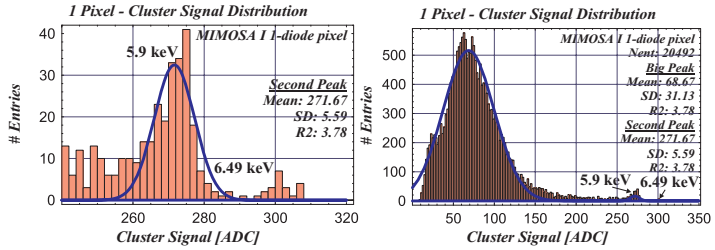


Figure 4. Calibrage absolu du circuit MIMOSA I avec des photons X de 5.9 keV.

La figure 4 présente les histogrammes de la spectroscopie des photons X pour évaluer le calibrage absolu de la chaîne de lecture. Le deuxième, petit pic correspond aux photons convertis dans la zone désertée d'une diode et représente 100% de l'efficacité de collection. Il est pris pour déterminer la valeur exacte du gain. L'efficacité de collection de la charge a été simulée en utilisant le logiciel ISE-TCAD. La figure 5 montre des résultats des simulations comparés à ceux obtenus expérimentalement avec des particules faiblement ionisantes.

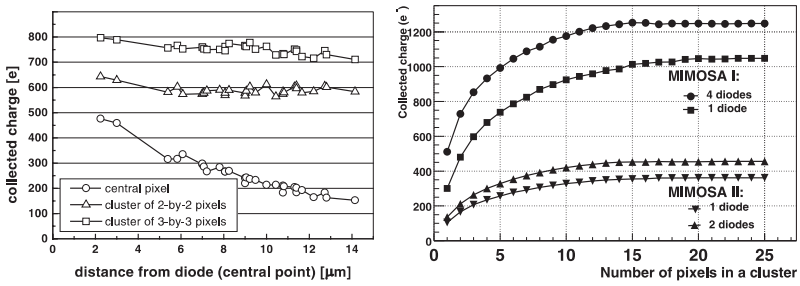


Figure 5. Efficacité de collection de la charge – un exemple des résultats simulés avec ISE-TCAD (à gauche), étalement de la charge obtenue au cours des mesures avec des particules de haute énergie.

La figure 6 présente les résultats de mesure de la résolution spatiale intrinsèque des capteurs CMOS. Les valeurs obtenues sont largement satisfaisantes pour un détecteur de vertex auprès du prochain collisionneur linéaire.

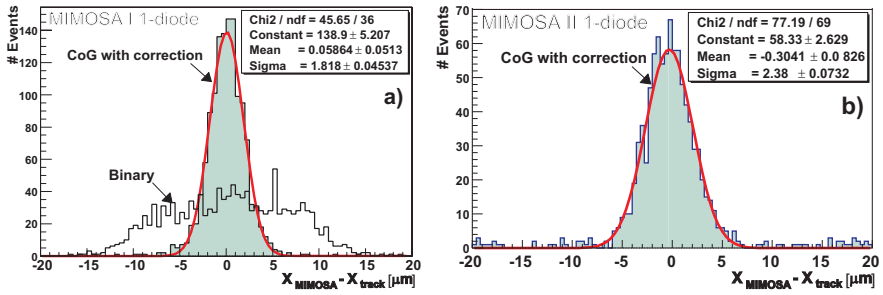


Figure 6. Distribution résiduelle de la position d'une trace mesurée par la matrice de pixels avec une seule diode de collection pour le prototype MIMOSA I, en utilisant deux algorithmes d'analyse donnant la résolution spatiale binaire et centre de gravité avec une correction non-linéaire -a), distribution correspondante pour le prototype MIMOSA II –b).

Conclusions et perspectives

Dans cette thèse est présentée la conception d'un capteur monolithique à base d'une structure classique à trois transistors pouvant être utilisée pour la détection des particules faiblement ionisantes. Des nouvelles structures du pixel sont aussi proposées comme par exemple une architecture avec mise à zéro automatique présentée dans la figure 7.

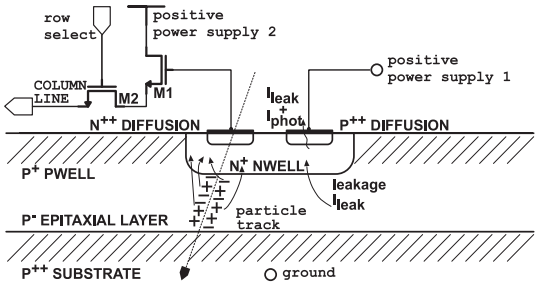


Figure 7. Principe de fonctionnement d'un pixel avec mise à zéro automatique.

Pour conclure, l'avantage majeur d'un détecteur monolithique à pixels actifs réalisé en technologie standard CMOS est son champ d'applications vaste et diversifié. L'aspect multidisciplinaire de ce genre de dispositif, et le grand intérêt commercial pour l'imagerie en lumière visible vont stimuler la recherche future vers des technologies mieux adaptées, offrant plus de souplesse pour la conception. Les technologies récentes de fabrication des circuits intégrés comprennent des possibilités d'intégrer le détecteur et son électronique sur le même substrat. De l'emploi possibilités s'ensuit un dispositif performant. Généralement, le développement d'une technologie spéciale dédiée à la fabrication d'un dispositif est coûteux

et les conditions en laboratoire ne garantissent pas la stabilité du processus. Au contraire, l'utilisation d'une technologie standard peut garantir un bon rendement, donc la réussite du projet. La communauté de la Physique Expérimentale de Haute Énergie peut donc profiter des développements des technologies industrielles avancées pour concevoir des systèmes de grande précision pour la détection et la trajectographie des particules.

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Chapter 1

INTRODUCTION

The human eye perceives the world by detecting scattered visible light, which has wavelengths in the neighbourhood of 500 nm. That is small enough not to be concerned by the wave characteristics of visible light, translating to the wavelength-resolution problem, since we do not look at things that are 500 nm wide. The details that can be resolved are limited by the wavelength of the radiation. In optical microscopes, objects down to the size of a living cell are investigated. To probe the tiny structure of matter down to smaller scales, the probe's wavelength has to be made smaller.

All particles have wave properties and according to de Broglie there is an inverse relationship between the de Broglie wavelength of a particle λ and its momentum p according to the formula $\lambda = h/p$, where h is the Planck constant and c is the speed of light. To penetrate the interiors of atoms and molecules and resolve atomic constituents, it is necessary to use radiation of a wavelength much smaller than atomic dimensions. The energy of the probing particle must be high. In electron microscopes, the atomic and molecular structures of matter down to the tens of nanometers scale are unravelled, with typical energies of electrons used of tens keV. However, the energy thousand times higher is needed to penetrate deeper into the structure of matter. Thus, particle accelerators are used to increase the momentum and energy of a probing particle and to decrease its wavelength. Accelerators, besides being a ultra-precision subatomic microscopes, where information is gathered from the analysis of scattering images of probing particles, are also being used to create new elements of matter in inelastic collisions of accelerated particles. The new particles are created by conversion of an excess kinetic energy from the collision energy into the mass.

1.1 Experimental Methods

In current high-energy physics experiments, particles are accelerated to high energies, and then forced to collide either with one another or with a stationary target. Most of the today's physics experiments aiming at probing deeper into the elementary constituents of matter are

using head-on colliding beam machines. In this case, all the beam energy is available for mass production and is not lost to the movement of the centre of the mass system for conserving momentum, as in fixed target experiments. When high-energy particles collide, numerous particles are created in such collisions. Quarks originating in the primary interactions hadronize within typical distances of a few fermi* from the interaction point resulting in many hadrons produced. Hadronization of quarks yields jets of particles, which retain the direction and energy of the parent parton. The visible final state is constituted only by stable hadrons. Reconstruction of the quarks' parameters, like momentum and energy, is obtained from the measurements of hadronic jets properties. Most of the hadrons decay immediately, but their decay products are detected. Many of them disintegrate after traversing short distances of a couple of hundreds of micrometers at a speed close to the speed of light. The distance traversed by a particle from the point of its creation to the its disintegration point is given by a product of c, τ and γ, where c is the speed of light, τ is the lifetime of a particle and γ† is the relativistic parameter defining the boost of the particle. The lifetimes of short lived and heavy particles interesting for physics processes are very short. As example, the lifetimes of bottom mesons B^0 and $B^{\pm}$, constituted of the bottom quark b, are correspondingly $(1.548 \pm 0.032) \times 10^{-12}$ s and $(1.653 \pm 0.028) \times 10^{-12}$ s. The lifetimes of charmed mesons D^0 and $D^{\pm}$, constituted of the charm quark c, are $(0.4126 \pm 0.0028) \times 10^{-12}$ s and $(1.051 \pm 0.013) \times 10^{-12}$ s, respectively. Many physics channels like Higgs, Z^0, SUSY particles, etc. are characterised by large decay branching ratios to heavy quarks and leptons. An example of a heavy lepton, exhibiting such strong coupling in these production processes, is the lepton τ with the lifetime amounting to $(0.2906 \pm 0.0011) \times 10^{-12}$ s. The respective decays and the type of the decaying particles are distinguished by measurements of impact parameters‡ for tracks of products originating in secondary and tertiary vertices close to the interaction point. The method based on reconstruction of the hadronic decays of heavy mesons or detection of their detached decay

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* 1 fermi = 10^{-15} m.

† $\gamma = 1/\sqrt{1-(v/c)^2}$, where v is the speed of the particle.

‡ The impact parameter is defined as the distance of the point of closest approach of the particle track to the interaction point.

vertex allows identification of the parent particles including determination of the flavour of the quark. This capability, consisting in an indirect tagging of the flavour of disintegrating particles, is provided by a vertex detector in an experiment.

Millions of particle collisions occur every second in current high energy physics experiments. Thus, sophisticated systems are used to track the particles and their properties as they fly away from the interaction point. Measurements of particle properties include track direction, charge, energy, momentum and mass and flavour identification. Different experiments at particle colliders look similar, since they perform similar measurements. The typical detector of a colliding-beam experiment is cylindrical, since particles may radiate in all directions and it consists of several layers used for different purposes. As an example, Figure 1-1 shows the view of one quadrant of the detector to be constructed at the TESLA experiment [1]. The whole detecting system features angular φ symmetry around the beam line axis sketched to the interaction point as passing from the right to left side.

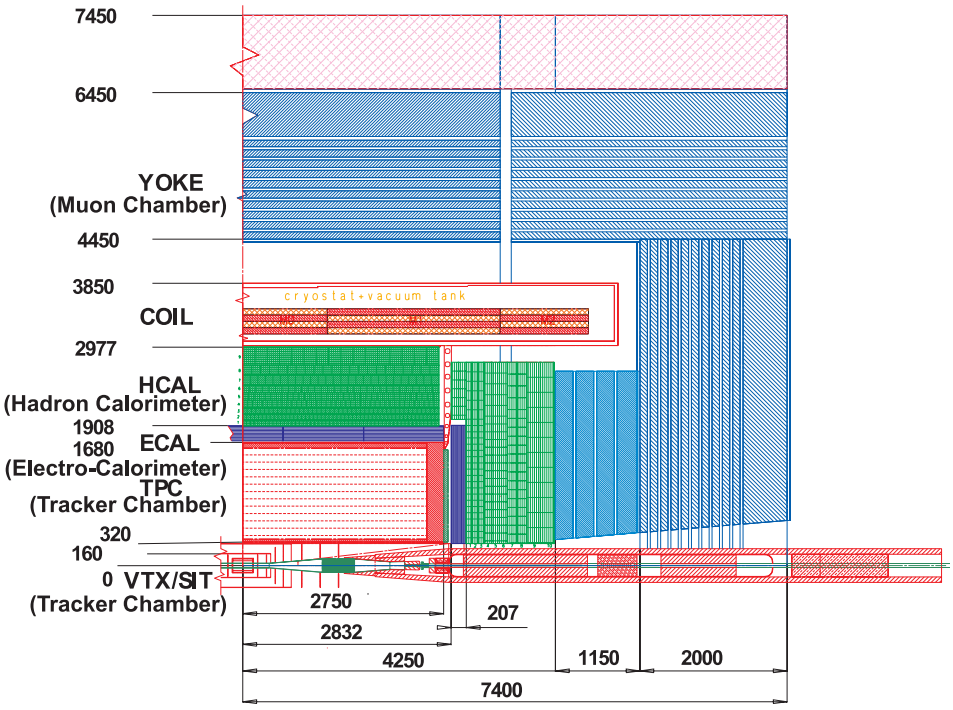

Figure 1-1: View of one quadrant of the TESLA detector (dimensions are in millimetres).

The innermost part of the detector in Figure 1-1 is constituted by a vertex detector, with the goal to reconstruct precisely secondary short-lived particles traversing only a few hundred microns from the interaction point before disintegration. It is placed closest to the beam

pipe, usually extending at the radius from 2 cm to 20 cm. It reconstructs the tracks of particles with a very high accuracy*. The vertex detector is built in the form of several concentric cylindrical layers of the detector plane of high granularity. Each detector planes enclosing the beam pipe consists of a few detecting slabs of multi-channel sensors, which are connected to the front-end electronics. The sketch in Figure 1-2 demonstrates the principle of a generic vertex detector installed on a e^+e^- collider. The detector is built close to the interaction point, and it is used for reconstruction of primary, secondary and tertiary vertices and complex jet topologies. In the inset to Figure 1-2, the definition of the impact parameter is also illustrated. The tracks from particular decays emerge from the secondary vertices. The measurement of impact parameters of particle tracks allows correlating the tracks with decay vertices and identifying the parent particle.

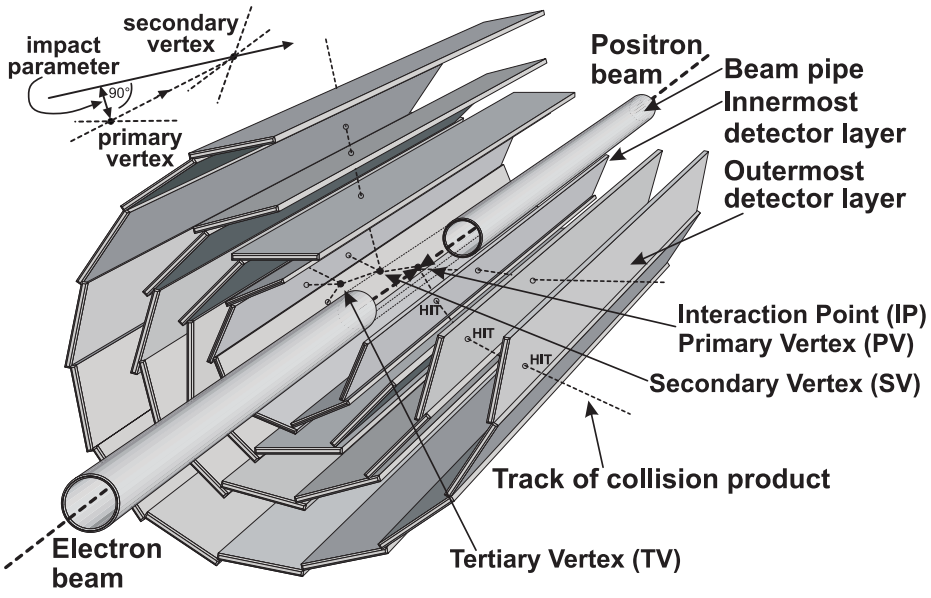

Figure 1-2: Conceptual design of a generic vertex detector comprising several layers of microstrip or pixel detectors. The definitions of the primary and secondary vertices are equally presented.

The vertex detector enables the detection of very short-lived fragments by reconstructing their trajectories close to the primary vertex. It identifies points of origin of particles in the form of secondary, tertiary vertices, different from the collision point, by distances corresponding to the particle lifetimes of only a few hundred of micrometers away. This allows studying important topics in modern particle physics, which is the physics of heavy

* The future collider experiments will require single plane spatial resolution in the order of a few micrometers.

quarks, i.e. Charm, and Bottom and the physics of Tau leptons.

The measurement of the impact parameters of charged tracks results an efficient flavour tagging. Recent experiments have profited enormously from investments in excellent vertex detectors. To illustrate the usefulness of these detectors, as an example, the event of a Z^0 particle decay reconstructed in the vertex detector of the ALEPH experiment is shown in Figure 1-3. The decay of a heavy B meson, originating in hadronization of Bottom quarks from an Z^0 decay, into lighter D meson, which decays further in kaons and pions constituted of light quarks, is shown.

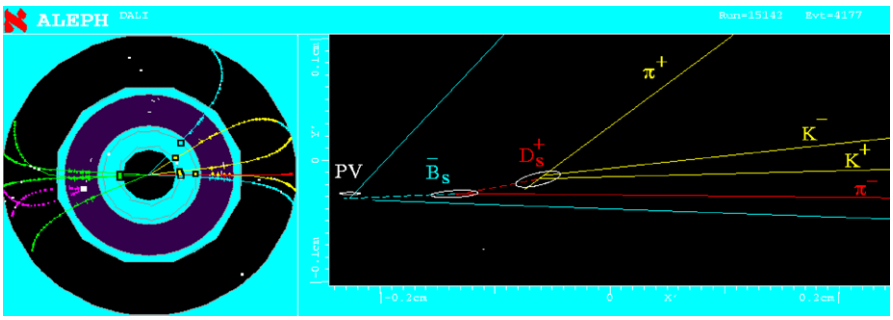

Figure 1-3: Typical ALEPH $Z^0 \to b + \bar{b}$ event showing the need for powerful vertexing capability (from ALEPH experiment).

In order to measure the impact parameter of tracks originating in secondary vertices the trajectories have to be precisely determined in all three dimensions, so it requires the use of several detector layers to allow precise extrapolation of tracks. The precision of the impact parameter determination in the case of a presumed two-plane vertex detector is given by

$$\sigma_{IP} = \frac{r_1\sigma_1 + r_2\sigma_2}{(r_2 - r_1)^2}, \tag{1-1}$$

where r_1, σ_1, and r_2, σ_2 are the detector layer radius and the single plane spatial resolution for the inner and outer detector layer, respectively. The requirement of a good lever-arm extrapolation implies an inner detector layer placed at the smallest possible radius around the beam pipe.

Recognising events, rich in heavy-quarks, requires compact detectors, which can operate in regions of extremely high particle density close to the interaction point. In such regions, conventional one-dimensional tracking detectors, e.g. microstrip detectors described in Chapter 3.3.1, may be inadequate. For this reason, high granularity pixel detectors are often

used for equipping the vertex detectors. Those highly segmented detectors were developed to provide a true picture of the space points (x, y) at which the tracks cross each layer. The research work in this field is oriented to achieve pixel detectors of high spatial resolution linked to high-density track resolving capability, sufficient radiation hardness, high read-out speed and reduction of multiple Coulomb scattering effects.

The outer region to the vertex detector of the detector system in Figure 1-1 is a tracking chamber to accurately measure trajectories of charged particles. The tracking chamber is a highly segmented sensing device, which is for example a Time Projection Chamber (TPC) filled with a gas mixture to form an active medium. The tracking chamber is used for large volume particle tracking at high magnetic field of a few teslas, typically. In a typical collider or fixed target experiment, the charged particle trajectory is measured by determining points in space, corresponding to the particles intersecting detector layers in the tracking chamber*. The track of a charged particle curves in the magnetic field and the measured points are fitted to the expected particle path obtained in analytical computation. This trajectory, in the presence of the magnetic field $\vec{B}$ and in the presumed absence of any electric field, can be calculated from the equation of motion, which has a simple geometrical form in this case given by

$$\frac{d^2\vec{x}}{ds^2} = \frac{zq}{\left|\vec{p}\right|}\left(\frac{d\vec{x}}{ds} \times \vec{B}\left(\vec{x}\right)\right), \tag{1-2}$$

where x is a position in space of the tracked particle, s is a path length of the trajectory and the product zq is the particle charge. For a constant homogenous magnetic field, the solution of equation (1-2) is a helix with radius R. The fit to the intersection points of the particle trajectory with detector planes allows the determination of the particle momentum and the particle charge. The particle momentum p is calculated in the presence of a magnetic field according to

$$p \approx 0.3\, z\, B\, R \left(\sin\alpha\right)^{-1}, \tag{1-3}$$

where p is expressed in GeV/c, z is the charge of the incident particle in units of the electron charge and α is the angle between the direction of the particle velocity for any

* In the context of a tracking chamber and a vertex detector, the term "tracking" is sometimes used referring to both tracking and vertexing capabilities at the same time.

point tangent to the particle trajectory and the magnetic field $\vec{B}$. The radius of curvature of the trajectory R is measured as a projection in the plane perpendicular to the direction of the magnetic field. The momentum resolution achievable is mainly determined by the spatial resolution of the tracking devices and by multiple Coulomb scattering in media along the track of the particle. Therefore, the relative momentum resolution $\Delta p/p$ is given by the sum of the curvature error due to the finite measurement resolution and the curvature error due to multiple Coulomb scattering, according to the formula

$$\left(\frac{\Delta p}{p}\right)^2 = \left(\frac{\Delta p}{p}\right)^2_{res} + \left(\frac{\Delta p}{p}\right)^2_{ms}, \tag{1-4}$$

for which the definition of the multiple Coulomb scattering is given in Chapter 2.2.5. Special care is needed to minimise scattering effects for low momentum particles in order to achieve good momentum resolution. The measurement of the momentum of charged particles is accomplished by determination of the deflection angle, radius of curvature or sagitta of the trajectories of the particles. The track curvature is defined as the inverse of the curvature radius 1/R. A fit to the coordinates of N equidistant points in space on the detected track is usually used to estimate its value. The distribution of measurements of the track curvature is approximately gaussian. The momentum resolution, accounting for measurement error in the track curvature for N>10 measurements made along the particle trajectory [2], is estimated by

$$\left(\frac{\Delta p}{p}\right)_{res,1/R} \approx \frac{\sigma_{spat,r\varphi}\, p}{0.3\, z\, B\, L^2 \sin\alpha}\sqrt{\frac{K}{N+4}}, \tag{1-5}$$

In formula (1-5), L is the projected track length onto the bending plane, N is the actual number of points measured along the track, $\sigma_{spat,r\varphi}$ is the spatial resolution of the single detector layer in the plane perpendicular to the magnetic field. The parameter K is equal to 320 if a vertex constraint is applied giving an additional point at the origin of the track to improve the tracking accuracy. Otherwise, for a standalone tracking in the tracker chamber without a vertex constraint the parameter K is equal to 720. In the case of a large track density resulting in many ambiguities and for a medium spatial resolution of the tracker chamber, the tracking task is difficult without reference to the track behaviour elsewhere. Generally, a high resolution, highly segmented vertex detector can provide good origin of the

tracks, which helps the central tracking systems in obtaining good momentum resolution.

The momentum resolution accounting for the measurement error in the track curvature due to multiple Coulomb scattering occurring in the media is estimated by

$$\left(\frac{\Delta p}{p}\right)_{ms,1/R} \approx \frac{0.016}{0.3\beta B \sin\alpha}\frac{1}{\sqrt{LX_0}}, \tag{1-6}$$

where X_0 is the radiation length of the scattering medium. It is apparent that in order to maintain a fixed momentum resolution as L is reduced, it is required that X_0 must be increased correspondingly. The general trend met in today's experiments is to have the tracking length of the tracking chamber long, typically $L \geq 1\,\mathrm{m}$, with the magnetic field in the range between $2\,\mathrm{T}$ to $4\,\mathrm{T}$. Additionally, the performance of the detector can be improved by the reduction of the amount of material in that tracking length. Thus, thin detectors are preferred and for the most demanding applications, thinning down of the detector elements is necessary.

The outermost detectors in Figure 1-1 are muon chambers detecting muons, which apart of neutrinos are the only particles able to penetrate the massive inner part. Inside the muon chambers are placed hadron and electromagnetic calorimeters. The electromagnetic calorimeter measures the total energy of electrons, positrons and photons. These particles produce electromagnetic cascades of e^+/e^- pairs and photons in the calorimeter material. The number of e^+/e^- pairs produced is proportional to the energy of the particle initiating the cascade. The hadron calorimeters measure the total energy of hadrons, which interact with the nuclei of the dense material in this region, producing hadronic showers of charged particles. Again the number of these charged particles is proportional to the energy of the incident particle whose energy deposit can be measured in this manner.

1.2 Semiconductor Detectors

1.2.1 Materials and Electronics

Large central tracking systems and vertex detectors, described in Chapter 1.1, aim at the observation of transits of charged particles. For their construction, semiconductor detectors are extensively used in nowadays experiments. Semiconductor devices are employed in

nuclear and particle physics in many applications. While, silicon is undeniably the most widely used material for tracking devices whose construction is based on solid-state detecting medium. It has the advantage of room temperature operation and wide availability. Other semiconducting materials as germanium, gallium arsenide, cadmium-telluride or diamond are rarely used in high-energy physics for tracking, although, they are very popular in other domains. For example, germanium detectors are used for high-resolution gamma detection in nuclear physics and cadmium telluride devices are used in nuclear medicine for X-ray detection. Diamond detectors were discussed for charged particle detection in the harshest radiation environment of the LHC experiments. Properties of semiconductor materials of interest are summarised in Table 1-1. The numerical values are given according to [3] under normal conditions i.e. for temperature around 298 K and a pressure of 101.3 kPa.

Table 1-1: Parameters values for materials used for semiconductor radiation sensors.

Material	**Proton number Z [a.m.u]**	**Material density ρ [g/cm^{-3}]**	**Band gap E_g [eV]**	**Energy / eh pair W [eV]**	**Electron mobility μ_e [cm^2/Vs]**	**Hole mobility μ_h [cm^2/Vs]**	**Electron lifetime τ_e [s]**	**Hole lifetime τ_h [s]**	**Intrinsic carrier density n_i [cm^{-3}]**
C diamond	6	3.515	5.5	13	1800	1200	2×10^{-9}	2×10^{-9}	$<10^3$
Si	14	2.329	1.12	3.61	1350	480	5×10^{-3}	5×10^{-3}	1.45×10^{10}
Ge	32	5.323	0.67	2.98	3900	1900	2×10^{-5}	2×10^{-5}	2.4×10^{13}
GaAs	31.33	5.317	1.42	4.70	8500	450	5×10^{-8}	5×10^{-8}	1.84×10^{6}
CdTe	48.52	5.870	1.56	4.43	1050	100	1×10^{-6}	1×10^{-6}	$\sim10^9$

The principle of operation of a semiconductor detector is based on the collection of charge carriers on signal electrodes. The electrons and holes are generated in an ionisation process, when the charged particle loses part of its energy passing through the detector. The ionisation is related to the total energy loss of the particle passing through the device and is measured as the number of electron-hole (e-h) pairs produced in the detector and collected for each impinging particle.

The electric field within the active volume of the detector separates opposite sign charge carriers and allows their fast collection. The presence of a junction is required for low band gap material sensors in order to raise the resistivity and limit the leakage current at room temperature by forming a zone depleted from free charge carriers. The depleted zone of a reverse biased p-n junction with low leakage currents, resulting in low shot noise, is most

often used as the active volume for signal detection [4]. For other materials, like CVD* diamond, characterised by inherently very high resistivity the p-n junction is not required and only ohmic contacts are used [5].

Advances in integrated circuit technology had an enormous impact on high-energy physics experiments. Progressing miniaturisation of integrated read-out circuits and increasing complexity of an on chip signal processing capability† is strongly related to the decreasing feature size of newly developed VLSI‡ processes. The progress achieved in microelectronic industry led also to improvements of the detecting elements themselves. Particle detectors took benefit of the development of the high volume production of integrated circuits, which offered readiness towards batch fabrication, better controllability of each processing step, monitoring and repeatability of properties of the silicon material used for fabrication. These perfections imply higher integration factor matched with read-out electronics and better signal-to-noise ratio (SNR) for particle detectors, thus higher resolution is achievable for the detecting systems employing these new devices. The term spatial resolution refers the precision of localising a single particle track. More precisely, it is the square root of the variance of the conditional probability density function to get a signal in the position x when a particle crossed the detector at the position x' according to

$$\sigma\left(x'\right)=\sqrt{\int\left(x-x'\right)^2 r\left(x-x'\right)dx}\,, \tag{1-7}$$

where r(x-x') is a probability of having a signal in the position x for an impinging particle in the position x'. Related is the capability of a detector to separate the signals arising from two particles traversing the detector at close distances. This is called two-track resolution. In modern detector systems, spatial resolutions, at which particle tracks are localised, of a few micrometers become achievable due to the progress of integration of the read-out electronics and due to improved techniques interconnect the detecting element and the read-out chip. The most important improvement is done in reduction of space needed for a single

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* CVD stands for Chemical Vapour Deposition.

† Gordon E. Moore, *Chairman Emeritus of the INTEL CORPORATION Board,* is widely known for "Moore's Law," in which he predicted that the number of transistors the industry would be able to place on a computer chip would double every year. In 1995, he updated his prediction to once every two years. While originally intended as a rule of thumb in 1965, it has become the guiding principle for the industry to deliver ever-more-powerful semiconductor chips at proportionate decreases in cost. The fabrication price of a transistor approaches today 1×10^{-6} cents (USD).

‡ VSLI stands for fabrication technology of Very Large Scale of Integration circuits and is used in exchange with ULSI meaning Ultra Large Scale of Integration.

read-out channel. These days, all high-energy physics experiments make beneficial use of advanced integrated circuits designed in commercial CMOS or BiCMOS fabrication processes [6, 7]. Modern sub-micrometer fabrication processes are now commonly used in designs of front-end electronics for particle physics experiment. They offer high immunity to radiation and high compactness of the design. The latter results in a possibility of integrating complex functions for signal processing and read-out control directly in the front-end chips.

1.2.2 Motivation for Pixel Detectors

The term "pixel detector" describes devices with the detector elements subdivided into an array of independent cells. Each segmented electrode is called a pixel. This term stands for a *picture element* and historically was reserved for imaging devices in the visible light spectrum. Pixel devices, delivering true two-dimensional pictures, are of great inter-disciplinary importance, including scientific applications and consumer electronics products. On the other hand, microstrip detectors are inherently able to offer only one-dimensional position resolution, and their use is limited mostly to high-energy physics applications. The microstrip detector design aspects are described briefly in Chapter 3.3.1. The variety of pixel devices, given the sensitivity of silicon for visible light, is the core of the huge commercial market for camcorders and other electronic image capture devices. In particle tracking, pixel detectors are best suited to provide high granularity and unambiguous particle track reconstruction. Pixel detectors, so far used as vertex detectors in high-energy physics, employ silicon sensors in the form of Charge-Coupled Devices (CCDs) described in Chapter 3.3.3.3, and Hybrid Pixel Detectors discussed in detail in Chapter 3.3.3.2. CCDs for charged particle tracking are closely related to those used in video cameras while Hybrid Pixels Detectors are application-specific variants being developed particularly for the LHC experiments as elements of vertex detectors being compatible with very high track densities and with harsh radiation environment. Both types of detectors require separate front-end electronics, which has an important impact on some of their performance parameters, e.g. in terms of read-out speed, amount of material traversed by particles, fabrication yield, etc.

Pixel detectors, applying criteria commonly used in application for visible light detection, are generally classified as passive and active sensors. Active pixel sensors are those equipped individually with a first stage of signal amplification integrated directly within the pixel area.

This approach is advantageous since it makes it possible to perform some processing operations independently on each pixel before signals are transferred to the common processing blocks placed on the periphery of the detector or to the external off-detector units. In the case of passive pixel sensors, the pixels provide only charge collection capability and the sensed charge needs to be transferred through the common read-out lines to the processing circuitry placed outside the area of the pixel array. For allowing the charge transfer, each cell contains transistor switches. Alternatively, as it is the case of Charge Coupled Devices*, a system of properly biased metal gates, inducing potential wells in the detector bulk, is used to perform sequential charge transfers to the read-out node. The part sensitive to radiation, i.e. the detector, and the read-out electronics can be processed separately on different substrates, which are connected together during the whole detector system assembling. The front-end electronics and the pixel detector are fully separated in the case of pad detectors, which are another type of pixel detectors described in Chapter 3.3.3.1, or Hybrid Pixel Detectors. Whereas, the first stage of the of the read-out electronics is integrated on a detector in the case of CCDs. Due to the technological limitations, this solution is usually limited only to the block realising charge-to-voltage conversion and the remaining processing is implemented on a separate chip. The full integration of the read-out electronics and the detector is only achieved for monolithic pixel detectors†. In this case, both components are fabricated using a planar process, for which all steps are carried out on the same substrate.

Most implementations of pixel-based detectors feature extremely low values of the detector capacitance, seen at the input of the read-out electronics, enabling low noise operation of the first stage amplifier. This results in much smaller signals providing a satisfactory SNR. An efficient detection capability is possible exploiting active layers reaching level even more than 20 times thinner than the typical thickness of 300 μm in the case of microstrip detectors. Formerly, in using devices with thin active layers, it was habitual to leave them mechanically thick. Recently, thinned devices are postulated for High Energy Physics

* Some part of the read-out electronics, i.e. a charge sensing amplifier with Correlated Double Sampling (CDS) capability, can be integrated directly on the CCD detector.

† Since classical passive pixel sensors with transistor switches used for connecting the sensing element to the read-out lines are rarely met in practical applications, another classification distinguishes two classes of pixel detectors i.e. Charge-Coupled Devices and Active Pixel Sensors.

detectors taking advantage of the development of etching techniques and handling of such thin structures. This approach will result in a significant reduction of multiple Coulomb scattering improving the tracking performance.

A few planes of the pixel-based detectors are usually able to provide an unambiguous track finding capability, while the same number of planes comprising microstrip detectors, even of double-sided, cannot resolve a high density event topology. Pixel detectors offer granularity several orders of magnitude higher than a typical microstrip detector. This may accept higher hit densities before effects related to ambiguous hit position reconstruction and cluster merging start to affect the track reconstruction algorithm. For this reason, pixel-based vertex detector planes, described in Chapter 1.1, can be placed much closer to the interaction point, resulting in much better precision of event reconstruction. In practice, the majority of the tracks are generally rather low momentum. The measurement precision at the interaction region is mainly limited by multiple scattering in the traversed material, which includes also the beam pipe, rather than by the intrinsic precision of the detector planes. Under these conditions, the usefulness of the multilayer detector for physics is dependent on possibility of achieving a small inner layer radius, spacing between layers similar to that radius and the smallest possible thickness of each layer. All these requirements are within the scope of pixel-based detectors.

Radiation hardness is also in favour of a pixel detector with respect to microstrip detectors. For long-strip detectors, the limiting parameter is the increase of the shot noise due to the increased leakage current after irradiation. In this case, the signal can be overwhelmed by noise. On the other hand, for pixel detectors the "strip length" is reduced by about two orders of magnitude. Thus, the noise associated with the leakage current is correspondingly reduced making pixel detectors useful for application where extremely hostile radiation conditions prevail.

Certain future applications, and their experimental conditions lead to demanding design requirements. The solution consists in integrating the detecting elements with the front-end electronics on the same silicon substrate using standard, easily accessible CMOS process used for fabrication of integrated circuits. Devices following this principle have been yet proposed for commercial use for still photography and video applications at the beginning of 90's. They are called CMOS Active Pixel Sensors (APS). Originally, their performance lagged

behind those of CCDs, however, after many improvements during recent years, they serve now as cheap and powerful solutions for imaging systems and become viable competitors for CCDs (see for example [8]).

The goal of this thesis was to demonstrate the feasibility and the adequacy of this new technology for efficient detection of charged particles and the possibility to its use for the construction of a vertex detector in future linear collider experiments. As an example of the work done, Figure 1-4 shows a partial die microphotograph of the Monolithic Active Pixel Sensor (MAPS) detector proposed for a highly efficient vertex detector for future collider experiments. This is one of several prototypes of MAPS type detectors fabricated within this work.

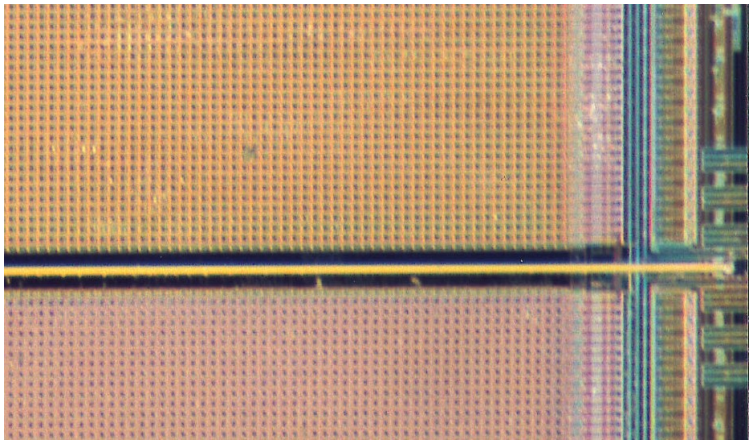

Figure 1-4: Partial die microphotograph of the Monolithic Active Pixel Sensor detector proposed for a highly efficient vertex detector for future collider experiments (MIMOSA I).

1.3 Constituents of Matter and Their Interactions

The "Standard Model" [9] describes the elementary particles and the forces by which they interact. It was built up through decades of intensive dialogue between theory and experiments. In this model, the elementary particles are divided into two classes, fermions, which have half integer spin and bosons, characterised by an integer spin. The bosons, to which the photon, the W^+, W^- and Z^0 particles and gluons belong, are carriers of the electromagnetic, weak and strong forces, respectively. The fermions are divided into two classes i.e. quarks and leptons, as it is shown in Table 1-2. Leptons and quarks are considered to be the fundamental constituents of matter. Quarks cannot be observed freely and always

have to combine to form hadrons in order to confine the gluon field (colour-force field) with other quarks.

Each particle has its corresponding anti-particle having the same properties except for opposite charge and opposite sign of some quantum numbers. There are four elementary forces whose characteristics are summarised in Table 1-3.

Electromagnetic and weak forces have been unified within the electro-weak gauge field theory. Quantum Chromodynamics (QCD) is the established theory describing strong interactions.

Table 1-2: Overview of the fermions according to the Standard Model.

Quarks						**Charge**
Up $m=1 \div 5$ MeV/c²	u	Charm $m=1.15 \div 1.35$ GeV/c²	c	Top $m=174.3 \pm 5.1$ GeV/c² m=168.2 +9.6, -7.4 GeV/c² (fit SM)	t	2/3 e
Down $m=3 \div 9$ MeV/c²	d	Strange $m=75 \div 170$ MeV/c²	s	Bottom $m=4.0 \div 4.4$ GeV/c²	b	-1/3 e
Leptons						**Charge**
Electron m=0.510998902 ±0.000000021 MeV/c²	e	Muon m=105.658357 ±0.000005 MeV/c²	μ	Tau m=1777.03 +0.30, -0.26 MeV/c²	τ	-1 e
Electron Neutrino m<3 eV/c²	ν_e	Muon Neutrino m<0.19 MeV/c²	ν_μ	Tau Neutrino m<18.2 MeV/c²	ν_τ	0 e

The familiar gravitational force acts on all particles with mass at any separation, but is so weak that it plays no role in sub-atomic physics. Hadrons are constituted of quarks, which are bound by the strong interaction. Hadrons are divided into baryons and mesons with half integer and integer spin, respectively. Baryons consist of three quarks, while mesons are formed by a quark-antiquark pair.

Table 1-3: Overview of the elementary forces according to the Standard Model.

Force	**Relative Strength**	**Distance Dependence**	**Particles "feeling" force**
Gravitational	10^{-45}	$1/r^2$	All (mass)
Weak nuclear	10^{-7}	short range (10^{-17} m)	All (weak charge)
Electromagnetic	1/137	$1/r^2$	Charged (electric charge)
Strong nuclear	10	short range (10^{-15} m)	Quarks (colour)

Examples of baryons are the neutron and the proton, constituted of one Up and two Down

quarks (udd) and two Up and one Down quark (uud), respectively. Examples of mesons are the pion and the kaon and the mesons D and B, which are composed of light and heavy quarks, respectively. Each quark has a baryon number of $1/3$ and three colour quantum numbers, while their corresponding anti-particles have a baryon number of $-1/3$ and the analogous anti-colour. Both neutron and proton have a baryon number of one, while all mesons are characterised by a baryon number of zero. It seems that in nature, only colourless states exist, i.e. mesons are colourless because for a quark-antiquark pair colour is combined with its corresponding anti-colour and baryons can also only be the colourless combination of three colour states.

In classical electrodynamics theory, the forces between particles are transmitted through a "field" filling the space. However, in quantum electrodynamics, the Einstein's equation, establishing equivalence between mass and energy ($E = mc^2$), combined with the Heisenberg uncertainty principle ($\Delta E \Delta t \geq \hbar/2$) provide an alternative description. The Heisenberg uncertainty principle allows particles to be created for a very short time even if no extra energy is available. For this very short time the uncertainty in the energy can be large enough to form so called virtual particles. The more energy is required for this virtual particle creation, the shorter the particle lifetime and its range are. Each particle is constantly emitting and absorbing such virtual particles, and if a virtual particle emitted by one particle is absorbed by another, then those two particles interact and the force between them is transmitted. In annihilation decay and processes, particles fuse into a very high-energy force-carrier particle, which almost immediately decays into low-energy particles. These high-energy, short-lived force-carrying particles can be created as real or virtual particles depending on the centre of mass energy available in the experiment. The virtual particles exist for such a short time that they can never be observed, but the products resulting from their decays can be identified in the final states of a given process. The real particles start to be created if the centre of mass energy $\sqrt{s}$ equals their rest mass energies. The principle of virtual particle generation in collision experiments is often used to examine properties of particles whose masses are beyond the total energy provided by the machine. However, certain physical channels can only be efficiently exploited at resonances providing the collision energy required to create the particle whose properties are

investigated. This approach motivates construction of machines of increasing collision energies, in which heavier particles can be analysed.

An example of a physical process passing through a virtual Z^{0*} or γ is the charmed mesons D production in an electron-positron collision through the annihilation process, $e^+ + e^- \rightarrow D^+ + D^-$. The flow of the process is shown in Figure 1-5. The annihilation of an electron-positron pair ends up with hadronization of quarks leading to high-density jets of secondary particles originating in further decays of mesons D.

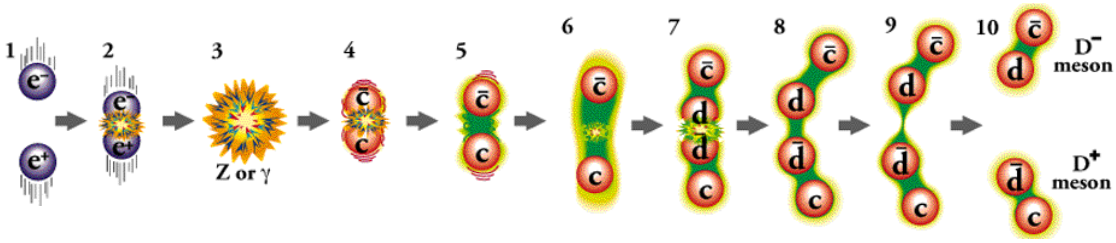

Figure 1-5: Layman view of the production process of charmed mesons D in electron-positron annihilation.

Each type of interaction has its own class of force carriers, which all are called gauge bosons. The heavier the force carrier is the shorter is its interaction range, and this is why the electric force is carried over the vast distances, as the mass of the carrier, the photon, is zero. The virtual carriers of the weak interaction, the W^+, W^- and Z^0 bosons, have masses around 100 times the proton mass explaining the shortest range of this type of interaction. The W and Z^0 bosons were discovered at CERN SPS collider. This discovery was a great success of the Standard Model, which formulated the unification of the electromagnetic and weak forces into one electro-weak interaction. The strong force carried by not freely existing gluons is limited by their self-interaction. Massless gluons carry colour force and couple to each other, confining the colour field lines to small distances. Owing to this fact, the range of the strong nuclear interaction is only 10^{-15} m. Gluons convert to particles with masses several hundred times the electron mass. The last, gravitational force is believed to be carried by gravitons, but despite a lot of experimental effort there is still no evidence for

* If the total energy of the annihilating electron-positron pair is equal to ~91 GeV in the centre of mass frame the Z particle in this process is real. Otherwise it is virtual. In the process, a charm quark and a charm anti-quark emerge from the virtual force carrier particle. They begin moving apart, stretching the colour force field between them. The energy in the force field increases with the separation between the quarks. When there is sufficient energy in the force field, the energy is converted into a quark and an anti-quark. The quarks separate into distinct, color-neutral particles: the D^+ (a charm and anti-down quark) and D^- (an anti-charm and down quark) mesons. The rest mass of the Z particle is 91.1882±0.0022 GeV/c^2.

their existence.

In the last few years many aspects of the Standard Model have been stringently tested, some to the per-mille level, with e^+e^-, ep and $p\bar{p}$ machines making complementary contributions, especially to the determination of the electro-weak parameters. With the data from LEP and SLC e^+e^- colliders, the measurements of the Z^0 boson became so precise that the mass of the Top quark was tightly constrained before it was directly measured in the Tevatron $p\bar{p}$ collider. After the Top quark discovery, LEP and Tevatron have extended the precision measurements to the properties of the W boson. These results, combined with neutrino scattering data and low energy measurements, provide an excellent concordance with the electro-weak part of the Standard Model. Despite these great successes there are many gaps in the understanding. One of them is electro-weak symmetry breaking which is related to the mass generation of gauge bosons and fermions*. These masses are generated in the Standard Model by the Higgs mechanism†. A new fundamental field, called the Higgs field, with non-zero vacuum expectation value breaks the electro-weak symmetry spontaneously. The W and Z bosons gain their masses by interacting with this field, while the photon remains massless; the same mechanism is responsible for mass generation of the quarks and leptons. The existence of a Higgs boson is not confirmed up to now. Although, some evidence for a Higgs mass signal at $m_{h_{SM}} = 115.0^{+1.3}_{-0.9}$ GeV with a significance of 2.9σ [10] was already reported by the LEP experiments. However, this is considered not enough to pretend a Higgs discovery. As an example, Figure 1-6 shows a recorded event with four jets $b\bar{b}q\bar{q}$ considered as a possible candidate for a Higgs particle generated through the Higgsstrahlung process [11] at the DELPHI experiment. The electro-weak sector of the Standard Model defines a 95% confidence level an upper limit slightly above 200 GeV/c^2 on

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* The weak and electromagnetic fundamental forces seem very different in the present relatively low temperature universe. But when the universe was much hotter so that the equilibrium thermal energy was on the order of 100 GeV, these forces may have appeared to be essentially identical - part of the same unified electroweak force. But since the exchange particle for the electromagnetic part is the massless photon and the exchange particles for the weak interaction are the massive W and Z particles, the symmetry was spontaneously broken when the available energy dropped below about 80 GeV and the weak and electromagnetic forces take on a distinctly different look. The model is that at an even higher temperature, there was symmetry or unification with the strong interaction, the grand unification. And higher still, the gravity force may join to show the four fundamental forces to be a single unified force.

† The theories attribute the symmetry-breaking to a field called the Higgs field, and it requires a new boson, the Higgs boson, to mediate it.

the Higgs boson mass. The Higgs particle discovery and its precise characterisation is one of the prime motivations to build new accelerating machines i.e. the Large Hadron Collider (pp - LHC) at CERN in Switzerland and the TeV-Energy Superconducting Linear Accelerator (e^+e^- - TESLA) probably at DESY in Germany.

Of course, the Higgs boson may not exist, but in that case some very valuable information could be obtained at those future colliders to develop a new theory, to explain the electro-weak symmetry breaking.

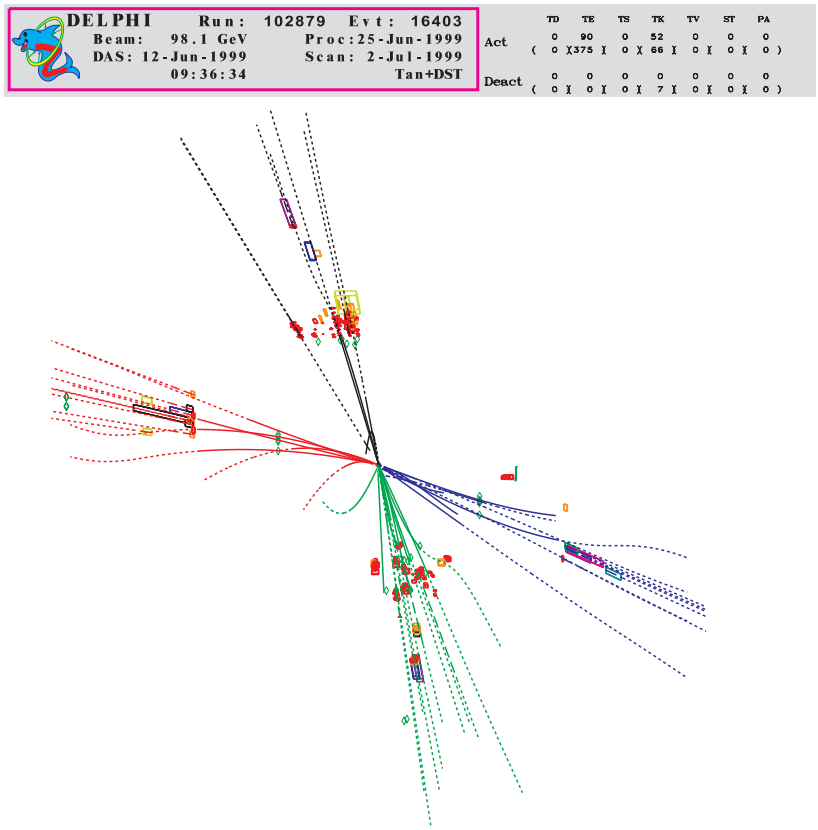

Figure 1-6: Four-jet event $b\bar{b}q\bar{q}$ at 200 GeV taken at the DELPHI experiment considered as a candidate for Higgs boson discovery (from DELPHI collaboration).

Several alternative scenarios are already developed for the physics, which may emerge beyond the Standard Model. This ranges from supersymmetric (SUSY) theories, which are well motivated theoretically and can incorporate a light Higgs boson to theories in which the symmetry breaking is generated by new strong interactions. Supersymmetry opens a new particle world in the energy range of the order from 100 GeV to 1 TeV. The new strong

interactions, a dynamical alternative to the fundamental Higgs mechanism, give rise to strong forces between W bosons at the TeV energy scale.

Dealing with the challenging physics issues will require new developments in detecting techniques and specific read-out electronics.

1.4 Requirements at Future Linear Collider (TESLA)

Considering optimisation of the detectors for future High Energy Physics experiments, four main detector benchmarks are concerned, i.e. track momentum resolution, jet flavour tagging, energy flow and hermeticity. The physics experiments at the future linear collider will demand optimal vertex detection. The physics calls particularly for high performance Bottom and Charm quarks flavour identification demanding pure and efficient tagging of secondary and tertiary vertices, and charge identification as needed for disentangling quark-anti-quark pairs[*]. Some physics processes to be studied will pass through several heavy quarks decays, complicating the reconstruction, and increasing the demand for highly granulated pixel detectors. The pixel-based detectors have already been used in numerous fixed target and collision experiments. The value of the pixel detector has been clearly established, even in the relatively clean physics experiments of the Stanford Linear Collider (SLC), where the mean pixel occupancy was a few times 10^{-5} for the beam-crossing interval of 8.33 ms and one full read-out carried in 25 beam crossings.

The resolution of the vertex detector is a convolution of the single point measurement precision, mechanical stability and multiple scattering effects. Even, at the high-energy collider (1 TeV), the average energy of particles in jets is expected to be in the region of 1-2 GeV. At the same time, the most interesting events will be characterised by high jet multiplicities. Thus, the detector design needs to be pushed to the limits of feasibility as regards the multiple scattering term and precision of point measurement. Optimal performance calls for point resolution better than 5 μm and thickness of the detector ladder under 0.2% of radiation length. The design of a vertex detector will be constrained by the

[*] Physics processes to be studied at future linear colliders and requiring ultimate vertex detector performance, include measurements of branching ratios of the Standard Model Higgs boson, investigation of various supersymmetry scenarios, such as supersymmetric Higgs searches in disintegration processes in τ leptons, improved measurements of the pair of W and Z bosons, the top quark studies, searches of the supersymmetric τ lepton, studying of the processes at the Z pole physics etc.

accelerator time structure and the expected radiation environment. Table 1-4 summaries main machine parameters and indicates some implications on vertex detectors for three considered construction of linear colliders, i.e. TESLA, Next/Japan Linear Collider NLC/JLC and the two beam acceleration scheme CLIC under study at CERN.

The diversity of physics signatures anticipated at TESLA and the characteristics of the bunch timing suggest a data acquisition scheme with continual readout having no trigger and no dead time for maximum data recording efficiency. The design of the TESLA collider is based on the concept of superconducting accelerating cavities working at medium frequency of 1.3 GHz [10]. The experimental conditions are moderate in terms of duty cycle, radiation level etc., compared to the LHC experiments, but are nevertheless quite demanding for the vertex detector design. The time interval separating two consecutive bunch-crossings (BX) within a bunch train (BT) will be 337 ns and 189 ns defining a duty cycle in the order of 0.5% for the BT repetition rate of 5 Hz and 3 Hz at a collision energy of 500 GeV and 800 GeV, respectively. The duty cycle foreseen allows to operate detectors only during beam crossing periods. Exploiting of the pulsed power mode of operation would allow reduction of the power consumption with most of the system being switched off between bunch trains. With increasing energy and bunch crossing rate, the detector environment changes. The number presented hereafter will refer to the TESLA parameters at the 500 GeV operation, unless it is stated explicitly.

Table 1-4: Linear colliders parameters.

Machine	$\sqrt{s}$ **[TeV]**	$\int \mathcal{L}$ **[$\times 10^{34}$cm^{2}s^{-1}]**	**Repetition rate [Hz]**	**Bunches /train**	**Bunch separation [ns]**	**Detector implications**		
						Layer 1 radius [mm]	**Hits* [mm^2 /BX]**	**Hits* [mm^2/ BT]**
TESLA	0.09...0.8	3.4...5.8	5...4	2820...4886	337...189	15	0.05	225
NLC/JLC	0.3...1.0	0.5...3.4	120	95...190	1.4...2.8	12	0.1	9.5
CLIC	1...5	11...15	150...50	154	0.7	30	0.005	0.8

* numbers are given for 0.5 TeV and 3 TeV operation of NLC/JLC/TESLA and CLIC, respectively, according to simulations which results may still evolves.

Detailed studies show that the dominated source of data volume in a vertex detector will be the beam background from e^+e^- pairs produced in conversion of beamstrahlung photons in the high electromagnetic fields of the colliding bunches. Another source of background will be due to the two-photon ($\gamma\gamma$) hadronic reactions. The two-photon collisions will

potentially be overlapping physics events, however the line between background and physics events will be decided during the experiment operation, and probably a considerable fraction of these events will be taken to for physics analyses. The most energetic two-photon collisions, i.e. with more than 2.2 GeV/c transverse momentum, are expected to result in the hit density of 3.4×10^{-5} hits for each BX per mm^2.

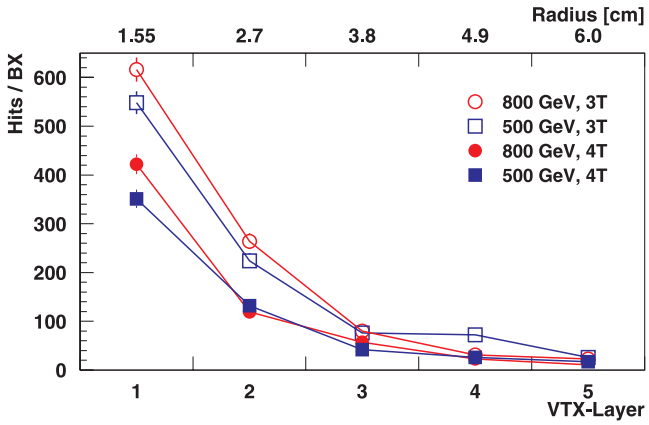

Figure 1-7: Number of hits resulting from pair background in the five layers of vertex detector for a magnetic field of 3 T and 4 T and for $\sqrt{s}$ of 500 GeV and 800 GeV (from TESLA TDR)

For the operation with the bunch crossing rate of 3 MHz for 1 ms followed by a period of almost 200 ms without any interaction, the event rate referred to the first layer of the vertex detector will be of the order of 600 hits per single bunch crossing. Figure 1-7 shows the number of hits resulting from pair background in the five layers of a vertex detector for a magnetic field of 3 T and 4 T and for the machine operation at the centre of mass energy $\sqrt{s}$ of 500 GeV and 800 GeV. The total hit occupancy, generated dominantly by e^+e^- pairs from beamstrahlung, is estimated to be about 0.6% for each 100 μs of the bunch train duration. Space and time ambiguities will therefore be difficult to resolve, especially since the number of hits from the physics processes is by more than two orders of magnitude less than that from background sources and the situation will be still complicated with high jet multiplicities. The hit rate due to the background in the first layer will dominate the total detector data rate translating into typically 10^6 pixels delivering data per single read-out. This contrasts with a number of pixels containing information useful for physics, which will rarely exceed an average value of 10^4. Compression of the data flow is therefore a major concern. The background has consequences on major vertex detector parameters, such as pixel size,

frame read-out speed, data flow compression, material budget and radiation tolerance, which are summarised hereafter.

The most complete vertex detector design was proposed for a vertex detector based on the CCD option [12]. However, MAPS or Hybrid Pixel Detectors can be used in very similar structures. The vertex detector would consist of five concentric layers with radii ranging from 15 mm to 60 mm covering the polar angles $|\cos\theta| < 0.96$ and $|\cos\theta| < 0.90$ for three inner and for the two outer layers, respectively. The four outer layers will allow stand-alone track reconstruction while the inner layer is essential for reconstructing track impact parameters to the interaction point as a crucial requirement of the TESLA vertex detector. This configuration will be adapted to the rather high occupancy expected in the first layer and it will enable internal alignment optimisation connected to rejecting background in the first layer.

The main constraint on the pixel size originates from the capacity to resolve neighbouring tracks inside the same jet and from the reconstruction accuracy on the impact parameter. These requirements are strongest for the layer closest to the interaction point and have to be considered leading to a trade off with the maximum number of read-out channels manageable by any data acquisition system. The experience on CCD devices, gained in their former application, led to a pixel size of approximately $20 \times 20\ \mu m^2$ in the case of the CCD based vertex detector option for TESLA. This pixel pitch is well adapted to the size of the clusters generated by high-energy particles in the CCD detector type. The charge spreading will also be large enough for this detector option to allow precise particle impact reconstruction via cluster charge distribution. Any charge weighting algorithms for data analysis, e.g. centroid fitting, can be used for this purpose. The accuracy required on measurements of impact parameter in the order of $100\ \mu m$ is the decisive factor for the study of τ and charmed particle decays. According to simulations, this implies already quoted spatial resolution of a single detecting plane of at least 5 μm and is easily achieved by CCDs. Taking into account similarities in charge collection mechanism between CCDs and MAPS, the same pixel size is affordable in the case of latter. The pixel size proposed, translates into a total number of approximately 800 millions of pixels for the complete detector. The number of pixels, which can be read out simultaneously, determines the read-out speed of the whole detector. The read-out speed can also be referred to as the

integration time of the signal. The read-out speed has to be calculated under the hypothesis that individual pixels will be read out serially shifted with a clock signal of the typical frequency equal to several tens of MHz. Practically, the maximum read-out clock frequency is considered up to 50 MHz, and this values is fixed taking into account that the maximum acceptable integration time will be dictated by the occupancy. The read-out speed results also from the achievable degree of subdivision of each detector ladder into streams, which could be read out, in parallel. In the case of CCDs, which realise the transfer of the charge from one extremity of the slab to the port where the front–end circuitry is placed, the maximum subdivision relies on parallel processing of columns arranged along the beam direction. In contrast to CCDs, MAPS detectors allow more flexibility. The charges are sensed, where they are collected, and the rows of sensing transistors are successively switched on by means of gating lines controlled by shift registers. The analogue signals are transmitted to the edge of the active area, where they can be processed. The columns processed simultaneously can be arranged along the shorter edge of the detector slab, i.e. transversely to the beam. The individual columns can be further subdivided into smaller parts or grouped to form sub-arrays. The configuration of the detector ladder proposed for the detector construction and the adapted read-out method should fully exploit advantage of possible random access to pixels. The proposed read-out scenario for the vertex detector consists in integration of signals over numbers of BXs, typically 60-300. The actual integration time, expressed in number of BXs, is initially determined by the prerequisite of the detector occupancy below 1%. The effective occupancy must take into account the cluster size due to the charge sharing, which increases it by one order of magnitude with respect to the actual particle hit rate. A high occupancy could be a potential source of hit confusion in the first layer, if the integration time of the sensors is not kept short enough. A typical integration time of 50 μs - 100 μs is considered, but it may need to be squeezed to 20 μs for the innermost layer of the detector. A high density of the hit pixels in the innermost layer may still be acceptable in this case, because of the standalone tracking performed with the four outer layers.

The mechanical support and the thermal control system may introduce a considerable amount of material that would degrade significantly the detector performance. The maximum amount of radiation length, which should be aimed for is typically 0.1% per layer. This requires thinning the sensors to a thickness well below 100 μm, possibly down to about

50 μm. It also necessitates the design of a particularly light but stable mechanical support. Finally, the thermal control or eventually the use of the cooling system requires a thorough study, which will depend on the best operating temperature for the sensors.

The radiation flux in TESLA has mainly two origins: the electromagnetic source which is composed of electrons and photons dominantly from beamstrahlung and the neutron gas due to interactions of particles in various beam elements and in the beam line surroundings. Simulations show that the vertex detector should be able to withstand an integrated electromagnetic radiation corresponding to 100 krad* in 5 years. During the same period neutron fluence of 1 MeV neutron equivalent close to 5×10^9 n/cm^2 is predicted, but a safety factor of 10 is postulated to be applied to these values in order to account for the limited accuracy of the simulations. The radiation hardness within the range of 100 krad is easily achievable with modern silicon technology, while the neutron fluence is acceptable with current CCD designs. However, it is questionable if there is scope for major improvements in their resistance to bulk radiation damage. In contrast to CCDs, the MAPS option has a large safety factor as regards their radiation tolerance.

* The unit rad is an unit of absorbed dose: 100 rad=1 Gy, where 1 Gy=1 J/kg.

Chapter 2

INTERACTION OF RADIATION WITH MATTER

2.1 Introduction

A fast, relativistic charged particle traversing matter loses energy in discrete amounts in independent, stochastic single collisions. It interacts with the electrons and nuclei of atoms. There are two principal features characterising the passage of charged particles through matter: the first effect consists in a loss of energy by the particle and the second one is a deflection of the particle from its incident direction. These two effects primarily originate from inelastic collisions with the atomic electrons of the material and elastic scattering from nuclei of the atoms. Different processes share the energy lost by the incident particle. The type of processes taking place in the traversed medium and the repartition of their contributions to the energy loss depend on the nature of the incident particles. The total energy loss is calculated as a sum of all contributions and the cumulative effect is observed.

Inelastic collisions with orbital electrons are almost exclusively responsible for the energy loss of heavy particle in matter. In these collisions, energy is transferred from the particle to the atom causing an ionisation by releasing the electrons or an excitation followed by light emission or relaxations observed as heat in the traversed material. Ionisation also includes discrete parts of the energy loss due to the δ-rays production* and other processes like the Møller and Bhabha scattering†. Production of δ-rays that are also called knock-on electrons, is related to some reactions, in which energy in excess of a few keV is transferred to a single atomic electron. Following the energy transfer, this electron itself causes a substantial secondary ionisation. In the case of heavy, charged particles, other energy losses than ionisation are marginal and are usually neglected.

For light charged particles, e.g. electrons and positrons, there are two main processes contributing to the continuous energy loss, i.e. ionisation and bremsstrahlung‡. The

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* The name dates back to the time of emulsions, when alpha and beta particles were also named.

† Møller and Bhabha processes refer to scattering of electrons on other electrons or positrons, respectively.

‡ Bremsstrahlung is the german word for radiation emitted under acceleration. In particular, the term is used for radiation caused by deceleration (braking radiation) when passing through the field of atomic nuclei.

bremsstsrahlung process is inversely proportional to the squared mass of the incident particle, thus it substantially accounts for radiation losses only for electrons. At electron energies above a few tens of MeV, bremsstrahlung dominates completely other processes.

The ionisation process is exploited for particle detection in solid state and gaseous detectors by a measurement of the generated charge. The detection technique usually consist in sweeping the freed charge carriers, which are e-h pairs in case of semiconductor medium out of the detecting volume by an electric field. As a consequence, the induced current signals are measured on the detector electrodes.

Radiation damage stands for the deterioration of the detection properties of a detector. Irradiation modifies the properties of the detector material, e.g. its crystalline structure or changes locally its electrical characteristic. The electronic circuits, assigned to read-out the detectors, are in the same way sensitive to radiation damages. Massive particles including neutral particles, e.g. neutrons, cause atomic displacements in the crystal materials and may initiate nuclear reactions with atoms of the traversed material. Dislocations of atoms from their normal sites in the lattice have long-term effects on semiconductor properties. They result from inelastic collisions of heavy particles* with atoms constituting the crystal lattice of the traversed material. Another group of radiation damage is caused by charged particles and photon interactions. The ionisation in the material accumulates and is followed by charged regions in insulators. This influences the active parts of detectors and electronics. However, the effect is reversible in some extent and usually anneals.

In order to improve clarity of the discussed material in Chapter 2.2, the complete summary of variables used in formulas quoted in this section, which includes also their definitions, is given in Table 2-5.

2.2 Interaction of Particles with Matter

2.2.1 Energy Loss of Heavy Charged Particles

Most reactions of heavy charged particles are electromagnetic elastic collisions with shell electrons in which the incoming particle losses energy. Charged particles, other than

* The most significant displacement damages may be caused by relatively low energy particles e.g. low energy protons below 10 MeV are characterised by the cross section for displacement damage in silicon several orders of magnitude higher than for higher energies.

electrons, lose energy in matter primarily by ionisation. One distinguishes between collisions where the energy transferred to the atomic electrons is large enough to extract them from the atom causing ionisation and collisions where the atomic structure is excited, without complete ionisation. In semiconductor materials, this effect gives rise to the mean value of the transferred energy, causing excitation of an electron from the valance band to the conduction band, higher than the band gap energy. In some reactions leading to ionisation, the amount of energy transferred is such that the electron itself causes substantial secondary ionisation. Elastic scattering from nuclei also occurs, but the energy transferred to the nuclei is negligibly small, since the masses of the nuclei of most materials (especially those used for constructing detectors) are large compared to the incident particles.

The inelastic collisions are statistical in their nature and occur with a certain probability. However, their number per macroscopic track length is generally large. Thus, the fluctuations in the total energy loss are small and a commonly used quantity is the average energy loss per unit track length $-dE/dx$. This quantity is expressed in $MeV/(g/cm^2)$*, representing the amount of energy loss per unit track length in a material of unit density. Following this approach makes the average energy loss per unit track length roughly independent of the material, as it is shown later in this chapter. The negative sign indicates that the moving particle losses energy.

The average energy loss can be derived, in the classical Bohr approach, considering the case of a particle of charge zq, passing a stationary charge Zq of the target particle at an impact parameter IP and velocity v, as depicted in Figure 2-1.

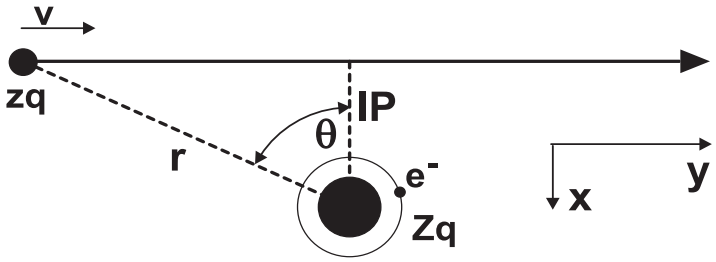


Figure 2-1: Collision of a heavy charged particle with an atomic electron.

Assuming that the moving particle passes the target so rapidly that the latter remains

* MKSA - system unit.

stationary during the "collision", the impact parameter IP will remain constant. In this case, the longitudinal electrostatic force exerted on the target before and after the moment of closest approach will cancel, leaving only transverse momentum transfer to the target. The impulse delivered to the target Δp is therefore calculated by integrating the effective transverse force and it is given by

$$\Delta p = \frac{Z z q^2}{4\pi\varepsilon_0 IP^2}\int_{-\pi/2}^{\pi/2}\cos^3\theta\,\frac{IP}{v\cos^2\theta}d\theta = \frac{Z z q^2}{2\pi\varepsilon_0 IP v} = \frac{Z z q^2}{2\pi\varepsilon_0 IP\beta c}. \qquad (2\text{-}1)$$

The calculations leading to formula (2-1) were performed non-relativistically. However, for the fast projectile particle, the longitudinal distance and the time are increased by a factor γ after applying Lorentz transformation into the coordinate system of the target particle. It can be shown that Δp remains unchanged after introducing relativistic corrections, thus expression (2-1) retains its validity also for moving relativistically particles.

Assuming, that the target of the mass m_T remains non-relativistic and does not move during the collision, it gains kinetic energy E_T according to

$$E_T = \frac{(\Delta p)^2}{2m_T} = \frac{Z^2 z^2 q^4}{2(2\pi\varepsilon_0)^2 IP^2\beta^2 c^2 m_T}. \qquad (2\text{-}2)$$

Due to the high difference in masses between the mass of a nucleus constituted of protons and neutrons and the mass of a shell electron m_e, it is reasonable to consider only the electrons as a possible target for the energy transfer. The energy transferred to the electron, expressed by equation (2-2), depends on the impact parameter IP.

The probability of having an energy loss of the magnitude between E and E+dE is given by the probability of an impact parameter between IP and IP+dIP. For a thin slice of material, of density ρ and thickness dx this probability is expressed by

$$P(E)dE = P'(IP)dIP = 2\pi IP\,dIP\frac{\text{number of electrons}}{\text{unit area}} =$$
$$= 2\pi IP Z\frac{N_A}{A}\rho\,dx\,dIP = \rho\frac{\pi Z N_A}{A}\frac{2z^2 q^4}{(4\pi\varepsilon_0)^2\beta^2 m_e c^2}\frac{dE}{E^2}dx\,, \qquad (2\text{-}3)$$

which includes all possible interactions with total number of electrons found in a slice of material of the thickness dx. Thus, the most probable energy loss per unit material density for particle traversing this slice is expressed by

$$-\left.\frac{dE}{dx}\right|_{loss} = \frac{1}{\rho}\int_{E_{min}}^{E_{max}} E\,P(E)\,dE = \frac{2\pi Z N_A z^2 q^4}{(4\pi\varepsilon_0)^2 \beta^2 m_e c^2 A}\left[\ln E\right]_{E_{min}}^{E_{max}}, \tag{2-4}$$

where E_{max} and E_{min} are the bounds on maximum and minimum energy which can be transferred to the target electron, respectively. The negative sign indicates that the moving particle loses energy. Using the relation between the transferred energy and the impact parameter, equation (2-4) can be rewritten as

$$-\left.\frac{dE}{dx}\right|_{loss} = 2C\frac{m_e c^2}{\beta^2}\frac{Zz^2}{A}\left[\ln IP\right]_{IP_{min}}^{IP_{max}}, \quad \text{with} \quad C = 2\pi N_A\left(\frac{q^2}{4\pi\varepsilon_0 m_e c^2}\right)^2, \tag{2-5}$$

Obviously, there are limits on IP_{min} and IP_{max} to prevent the value of the integral being infinitive. The upper bond on impact parameter is calculated requiring the collision time being "long" compared to the period of the electron in its atomic orbit, which yields

$$IP_{max} = \frac{\gamma\beta c}{2f_{rot}} = \left.\frac{\gamma\beta c h}{2I}\right|_{h f_{rot}=I}, \tag{2-6}$$

where I refers to the mean ionisation potential of the atom. In order to calculate IP_{min}, a proper quantum mechanical relativistic calculation is needed for the full result. An approximate solution can be given defining the minimum object size, which can be seen from the rest frame of the incident particle. Thus, IP_{min} is equal to the de Broglie wavelength of the relativistic particle, and is expressed by

$$IP_{min} = \frac{h}{m_e \gamma\beta c}. \tag{2-7}$$

Substituting limits given by equations (2-6) and (2-7) into equation (2-5) gives the following approximate expression for the mean energy loss

$$-\left.\frac{dE}{dx}\right|_{loss} = 2C\frac{m_e c^2}{\beta^2}\frac{Zz^2}{A}\ln\left(\frac{\pi\gamma^2\beta^2 m_e c}{I}\right), \tag{2-8}$$

which is the classical Bohr formula. It gives a reasonable description of the energy loss for very heavy particles such as α-particles. However, for lighter particles, the formula breaks down because of quantum effects. It contains, nevertheless all the essential features, of electronic collision energy loss by charged particles. The energy loss scales by z^2 of the incoming particle and is independent on its mass. It is also independent on the traversed material properties due to the nearly constant ratio Z/A for all most of materials. For slowly

moving particles with $\gamma\beta < 1$, the energy loss increases as $1/\beta^2$.

The full quantum mechanical treatment based on the momentum transfer rather than the impact parameter analysis yields the mean rate of energy loss (stopping power) given by the commonly used Bethe-Bloch [13] equation

$$-\left.\frac{dE}{dx}\right|_{loss} = K z^2 \frac{Z}{A}\frac{1}{\beta^2}\left[\frac{1}{2}\ln\left(\frac{2 m_e c^2 \beta^2 \gamma^2 T_{max}}{I^2}\right) - \beta^2 - \frac{\delta}{2}\right], \tag{2-9}$$

where T_{max} is the maximum kinetic energy that can be transferred to a free electron in a single collision. The parameter T_{max} is limited by conservation of energy and momentum and for an incident particle of mass M is expressed by

$$T_{max} = \frac{2 m_e c^2 \beta^2 \gamma^2}{1 + 2\gamma\frac{m_e}{M} + \left(\frac{m_e}{M}\right)^2}. \tag{2-10}$$

The parameter δ corrects for the density effect related to the polarisation of the medium. This limits the electric field of very fast charged particles, effectively truncating the logarithmic rise of the energy loss function (2-9) at very high energies for $\gamma\beta > 10$. The density effect correction is usually computed following Sternheimer's parameterisation [14], given by

$$\delta = \begin{cases} 0 & \text{if} \quad \left(\log_{10}(\gamma\beta)\right) < x_0 \\ 2(\ln 10)\left(\log_{10}(\gamma\beta)\right) - \bar{C} + a\left(x_1 - \gamma\beta\right)^m & \text{if} \quad x_0 \le \left(\log_{10}(\gamma\beta)\right) < x_1 \\ 2(\ln 10)\left(\log_{10}(\gamma\beta)\right) - \bar{C} & \text{if} \quad \left(\log_{10}(\gamma\beta)\right) > x_1 \end{cases}. \tag{2-11}$$

The quantities: x_0, x_1, $\bar{C}$, a and m in the equation (2-11) depend on the absorbing material and they are computed from the analytical fit of this expression to the experimental data. The values for different materials are tabulated in literature, those for silicon are as follows: $x_0 = 0.2014$, $x_1 = 2.87$, $x_1 = 2.87$, $\bar{C} = -4.44$, $a = 0.1492$ and $m = 3.25$ [15].

The energy loss by electrons and positrons is not described by equation (2-9). At low energies electrons and positrons primarily lose energy by ionisation. While ionisation loss rise logarithmically with energy, bremsstrahlung losses rise nearly linearly, and dominates above a few tens of MeV in most materials. Ionisation loss by electrons and positrons differs from loss by heavy particles because of the kinematics, spin, and the identity of the incident

electrons with the atomic electrons subjected to ionisation. Thus, energy loss by light charged particles requires a different description, and the collision energy loss contribution is given by the modified Bethe-Bloch formula [15]. The most important factor in energy loss by electrons and positrons is their small mass. For light charged particles, the modified Bethe-Bloch formula accounts for change in direction of the incident particle and assumes the maximum transferred energy in a collision to be half the kinetic energy of the incident particle.

The amount of charge liberated in the active volume of the detector, which contributes to the sensed signal, depends on the energy deposited along the particle track rather than directly on the energy lost by the traversing particle. In reality, some of the energy lost by a traversing particle is removed from the track vicinity and escapes from measurements. This energy is carried away by a few high-energy knock-on electrons produced or by fluorescence photons emitted by atoms and photons radiated by incident particles or in a much less extent by Čerenkov radiation. Practical detectors measure the energy, which is deposited close to the particle track, not the total energy lost. The Bethe-Bloch formalism quoted does not include energy loss due to radiation. However, when energy is carried off by energetic knock-on electrons, it is more appropriate to consider the mean energy loss excluding greater energy transfers than some cut-off energy T_{cut}. Thus, the mean restricted energy loss rate function is used. It describes the mean rate of energy deposited along the track in the detector according to the following formula

$$-\left.\frac{dE}{dx}\right|_{restr.} = K z^2 \frac{Z}{A}\frac{1}{\beta^2}\left[\begin{array}{l}\frac{1}{2}\ln\frac{2 m_e c^2 \beta^2 \gamma^2 MIN(T_{cut}, T_{max})}{I^2} - \\ -\beta^2\left(1+\frac{MIN(T_{cut}, T_{max})}{T_{max}}\right)-\frac{\delta}{2}\end{array}\right], \qquad (2\text{-}12)$$

where $T_{cut} \approx 140$ keV for silicon. The reported value of T_{cut} results from fitting the expression (2-12) to the experimentally measured values of the mean restricted energy loss in 300 μm thick silicon microstrip detectors [5]. The restricted energy loss smoothly joins the energy loss given by the normal Bethe-Bloch function for $T_{cut} > T_{max}$. The plot of stopping power for pions in silicon as a function of the ratio between the momentum of the slowing particle p and the particle mass M is shown in Figure 2-2. The graphs were evaluated according to equation (2-9) describing the mean energy loss without ($\delta = 0$) and with density

correction and equation (2-12) for restricted energy loss. Perceptibly, the stopping power in each medium decreases showing the inverse proportionality to β^2 for particle velocities for which occurs $\gamma\beta < 1$. The mean energy loss shows a minimum at $\gamma\beta \approx 3$. Particles with this minimum amount of the energy loss are called *Minimum Ionising Particles* (MIPs). The energy loss starts increasing proportionally to $\ln\beta\gamma$ instead of $\ln\beta^2\gamma^2$ from $\gamma\beta \approx 3$ upwards. This increase accounts for the correction for the density effect due to the media polarisation effect, which is given by equation (2-11). Despite nearly constant ratio Z/A for most types of materials, the stopping power increases slightly for low Z materials and decreases for high Z materials. This effect originates in different density parameter δ for various materials. For all practical purposes in high-energy physics, the stopping power in a given material is a function only of the velocity of the incident particle βc and the stopping power curves are about the same for different particles, e.g. muons, protons or pions with a minimum for $\gamma\beta \approx 3$. On the other hand, the density effect and the restriction of the maximum energy transfer become significant for ultra relativistic particles. The suppression of the relativistic rise of the Bethe-Bloch formula cancels the dependence of the restricted energy loss on the energy of the incident particle. The flat part of the distribution representing a minimum amount of the deposited energy along the track extends towards ultra high particle velocities.

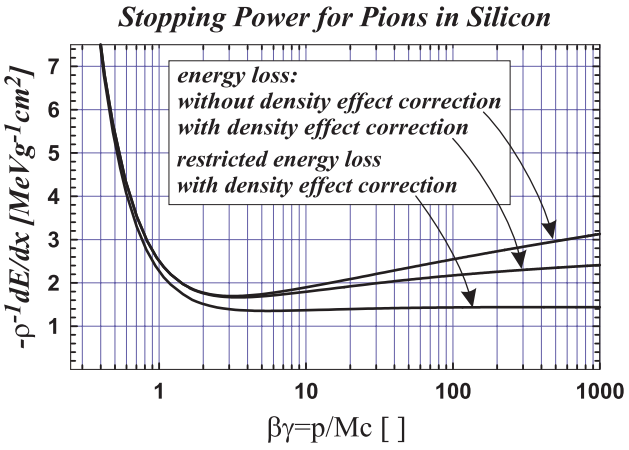


Figure 2-2: Stopping power for pions in silicon as a function of the ratio between the particle momentum p and the particle mass M.

The mean energy deposited in the detector, available for measurements, by a charged

particle travelling the distance x_{tr} is

$$\overline{E_{dep}}(x_{tr}) = \int_0^{x_{tr}} \left(-\left.\frac{dE}{dx}\right|_{restr.} \right) dx \approx x_{tr} \left(-\left.\frac{dE}{dx}\right|_{restr.} \right). \tag{2-13}$$

The approximation holds as long as $\gamma\beta > 3$, where the restricted energy loss rate is independent of the travelling distance in the medium. The value of the parameter T_{cut} allowing to fit the measured energy loss with expression (2-12) is obtained experimentally, and varies with the material properties and geometry of the detector.

Table 2-5: Summary of variables used in formulas introduced in Chapter 2.2.

Symbol	Value	Unit	Definition
$\frac{dE}{dx}$	-	$\left[eV\,g^{-1}\,cm^2 \right]$	Energy loss
K	0.307	$\left[MeV\,g^{-1}\,cm^2 \right]$	$4\pi N_A r_e^2 m_e c^2$
N_A	6.022×10^{23}	$\left[mol^{-1} \right]$	Avocado's number
r_e	2.818×10^{-15}	$\left[m \right]$	Classical electron radius
$m_e c^2$	0.510	$\left[MeV \right]$	Electron mass $\times c^2$
c	2.998×10^{8}	$\left[m\,s^{-1} \right]$	Speed of light in vacuum
z	-	-	Charge of incident particle
Z	for silicon Z=14	-	Atomic number of medium
A	for silicon A=28.0855	$\left[g\,mol^{-1} \right]$	Atomic mass of medium
v	-	$\left[m\,s^{-1} \right]$	Incident particle speed
β	v/c	-	Relative particle speed
γ	$1/\sqrt{1-\beta^2}$	-	Relativistic dilatation factor
T_{max}	32	$\left[MeV \right]$	Maximum energy transfer
I	$\approx 16\,Z^{0.9}$ for silicon I=Si: 172	$\left[eV \right]$	Excitation potential per atomic electron
$\frac{\delta}{2}$	$\approx \ln\left(\frac{\hbar\omega_p}{I}\right) + \ln(\beta\gamma) - \frac{1}{2}$ at very high energies	-	Density effect correction
$\hbar\omega_p$	$28.816\sqrt{\rho\left(\frac{Z}{A}\right)}$	$\left[eV \right]$	Plasma energy
M	-	$\left[MeV/c^2 \right]$	Incident particle mass

2.2.2 Fluctuations in Energy Loss

The quantity $(dE/dx)\delta x$ represents the mean energy loss via interaction with electrons in a layer of the medium characterised by the thickness δx. For finite δx, there are fluctuations in the actual energy loss. The amount of energy loss is a stochastic quantity with two sources of variations i.e. the amount of energy transferred in a single collision varies and the actual number of collisions. The number of collisions fluctuates according to the Poisson law i.e. for N collisions the number of collisions varies as $\sqrt{N}$. The relative variation of the collision number is inversely proportional to $\sqrt{N}$, so in the limit of very thick absorbers, the fluctuations in the energy loss due to the number of collisions vanish. However, for a finite thickness medium, the actual value of the collision number fluctuates. The distribution of the energy loss is called the *straggling function*, and only for a thick layer it has a nearly gaussian form. The thickness limit is defined by imposing the following condition upon the mean energy loss: $(dE/dx)\delta x \gg T_{max}$. In general, the distribution is non-symmetric, skewed towards high values, with a long tail in the direction of high values of energy depositions. The probability of individual interactions with large amounts of energy transferred is strongly reduced, which implies the mean value of the distribution higher than the most probable one. A detailed description of energy loss straggling in thin silicon devices can be found in the reference [16]. The first description of the energy straggling function was given by Landau [17], where three assumptions were made: the most important assumption allows infinite energy transfers by transferring all the energy of the incident particle to a single shell electron, the second postulation assumes the shell electrons as free carriers and the last one makes the particle velocity not affected by the passage through the detector. The last statement is only true if the absorber of the total thickness x is thin. This means that the mean energy loss is small compared to the maximum energy transferred per single interaction T_{max}, which can be expressed by

$$\rho K z^2 \frac{Z}{A}\frac{1}{\beta^2} x << T_{max}. \qquad (2\text{-}14)$$

For example for 120 GeV/c pions traversing a silicon detector, equality in condition (2-14) occurs for a 12 cm of the detector thickness. Thus, the condition for a thin absorber is satisfied for all detectors, which are much thinner than this value. The Landau's straggling

function can be used to fit the measured energy loss spectra, which are always a convolution of the actual energy loss straggling function with distributions due to other processes (e.g. noise, partial charge collection efficiency, etc.). The fluctuations are smaller for the restricted energy loss rate given by equation (2-12). The Landau function is approximated by the following normalised distribution [18]

$$\Phi(\lambda) = \int_{-\infty}^{\lambda} \phi(\tau)\,d\tau, \text{ where } \phi(\lambda) = \frac{1}{2\pi i}\int_{-i\infty}^{+i\infty} e^{(\lambda s + s\ln s)}\,ds \text{ and } \lambda = \frac{\left(N_{gen} - N_{mp}\right)}{\Delta_{FWHM}} q, \qquad (2\text{-}15)$$

where $\Phi(\lambda)$ is the distribution integral function of $\phi(\lambda)$ which refers to the probability density of having a particular amount of charge generated, and the parameter λ is a dimensionless number proportional to the energy deposited. The measured values for the most probable amount of charge generated $N_{mp}q$ and the width (FWHM*) Δ_{FWHM} of the Landau distribution have to be used in order to derive the distribution of signals i.e. the probability density function of a specific number $N_{gen}q$ of charge carriers generated. Figure 2-3 shows a typical distribution defining the probability of having a collision with a given energy transfer in a thin absorber.

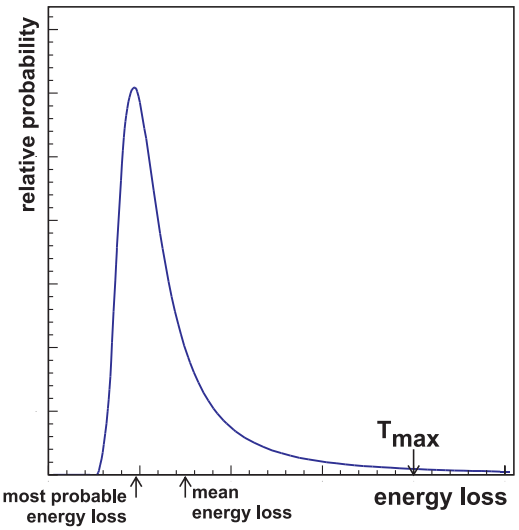


Figure 2-3: Typical distribution of energy loss in a thin absorber given by Landau distribution function.

The mean energy loss does not correspond to the peak, but is displaced because of the presence of the high-energy tail. The position of the peak defines the most probable energy

* FWHM stands for Full Width at Half Maximum and addresses the width of a distribution of measured quantities.

loss.

When the mean energy required for charge carrier generation in a given material is known, the most probable energy loss allows to define the most probable number of charge carriers generated along the particle track per unit length. In the case of semiconductor material this quantity is expressed in the number of e-h pairs generated. A single MIP particle yields about 76 e-h pairs per micrometer of the particle track as the most probable number in a detector made of silicon.

2.2.3 Energy for Charge Carrier Generation in Semiconductor Material

The energy W required to create an e-h pair in a semiconductor by a fast, charged mass particle traversing the medium depends on the band gap energy E_g of the material and hence, although only slightly, on the temperature. The measurements of this quantity show a nearly linear dependence on the band gap energy, and the linear fit to the data obtained for different materials gives [19]

$$W\left(E_g\right) = 1.76\,[\mathrm{eV}] + 1.84 \cdot E_g\,[\mathrm{eV}]. \tag{2-16}$$

The energy for charge carrier generation is always higher than the band gap energy due to the possible additional excitation of phonon and plasmon states. Phonon excitation transfers energy to the lattice, and the energy transferred appears finally as heat in the detector. The plasmon is the quantum of the valence electron density oscillations with a mean energy of 17 eV for silicon. The valence electrons are those of the M-shell and they are only weakly bound to the atoms. Thus, they may be considered as a dense and nearly homogeneous density gas, i.e. plasma of negative charge carriers in the semiconductor material volume. The plasma of valence electrons is immersed in a fixed positive charge distribution of atoms bound in the crystal lattice. The traversing particle or impinging high-energy photon generates the density oscillation states in this medium. Thus, the plasmon is recognised as a state of the real or virtual photon coupled to the valence electron plasma. The plasmons deexcite almost entirely by an e-h pairs creation. The freed charge carriers convey the plasmon energy and can be somewhat energetic. They are referred as "hot carriers". Like the δ-electrons produced in close collisions, they lose energy by further phonon excitation and ionisation. The mean energy W to create an e-h pair has been calculated and measured in experiments including high-energy charged particles and X-ray photons [19, 20]. The mean

energy W required to create an e-h pair in silicon is $W \approx 3.6\ \text{eV}$ [*].

2.2.4 Radiation Length

Energy loss due to radiation emission is negligible for heavy particles with masses significantly higher than the mass of the electron. However, a high-energy electron or a high-energy photon incident on matter initiates electromagnetic cascades by bremsstrahlung and e^+e^- pair production processes, respectively. The characteristic amount of matter traversed for these related interactions is called the *radiation length* X_0, which is usually measured in g/cm^{-2}. This is a scaling variable used for the probability of occurrence of bremsstrahlung or pair production, and for the variance of the angle of multiple Coulomb scattering (Chapter 2.2.5). The average energy loss due to bremsstrahlung for an electron of energy E is related to the radiation length by

$$\frac{dE}{dx} = \frac{1}{X_0} E \quad \Rightarrow \quad E(t) = E_0 e^{-\frac{t}{X_0}}, \tag{2-17}$$

where E_0 is the initial energy of the incident particle. Thus, the radiation length is a mean distance over which a high-energy electron losses all but $1/e$ of its energy by bremsstrahlung. The probability for a e^+e^- pair to be created by a high-energy photon equals to $\frac{7}{9} X_0$. The value of radiation length depends on the atomic number Z of the material. A useful approximation convenient for quick calculations of the radiation length is given by

$$X_0 = 716.4 \frac{A}{Z(Z+1)\ln\left(287/\sqrt{Z}\right)}. \tag{2-18}$$

Equation (2-18) is a heuristic expression providing 2.5% agreement with more accurate and advanced estimations. The radiation length for silicon is $X_0 \approx 9.36 \cdot \rho_{Si}\ \ g/cm^{-2}$. The radiation length in mixtures or compounds of materials having different properties is calculated as a weighted mean of contributions from each constituent.

[*] Photons from visible light spectrum undergo internal photo-electric generating single e-h pair in semiconductor material. The energy of generated carriers is not sufficient to result in further ionisation. Thus, the energy required to create single e-h pair for visible light photons is equal to the energy gap of the material amounting to ~1.12 eV for silicon.

2.2.5 Multiple Coulomb Scattering

A charged particle traversing a medium is deflected by many small-angle scatters. Most of these deflections result from repeated Coulomb scatterings from nuclei. Hence, the effect is called multiple Coulomb scattering. The angular distribution of outgoing tracks projected onto a plane relative to the incident tracks depends on the detector thickness x, the radiation length of the detector material X_0 given by equation (2-18), the particle velocity β, the particle momentum p and its charge number z. The Coulomb distribution scattering is roughly gaussian for small deflection angles. Thus, for most application, the use of a gaussian distribution with a standard deviation of

$$\Theta_0 = \frac{13.6\ \text{MeV}}{\beta c p} z \sqrt{\frac{x}{X_0}} \left[1 + 0.038 \ln\left(\frac{x}{X_0} \right) \right] \qquad (2\text{-}19)$$

is sufficient. Scatterings at larger angles are more probable for low momentum particles than particles with the high momentum. However, at larger angles, greater than a few θ_0 defined by equation (2-19), the distribution has much larger tails than does a gaussian distribution. The value of θ_0, given by equation (2-19), results from a fit of a gaussian distribution function to the distribution obtained according to more accurate theory for singly charged particle with $\beta = 1$ and for all atomic numbers of the traversed materials. It is accurate to 11% or better for x/X_0 in the range $10^{-3} < x/X_0 < 100$. Since the standard deviation of the scattering angles, given by equation (2-19), describes the angular distribution projection onto a plane, the standard deviation in space is $\sqrt{2}\,\Theta_0$.

Equation (2-19) describes scattering from a single material, while the usual problem encountered in practice involves the multiple scattering of a particle traversing many different layers and mixtures. In order to find precisely the result for the combined scatterer, it is much more accurate to apply equation (2-19) once, after finding x and X_0. Otherwise, the result is systematically too small due to the cut of long tails of the real distribution resulting from a Gaussian fit.

Multiple scattering effects may significantly affect the precision of a vertex detector. The figure of merit for any vertex detector can be expressed by the precision with which one measures the track impact parameter (IP), separately in the radial and longitudinal directions.

For a set of cylindrical detectors, this resolution can be expressed as

$$\sigma_{IP} = \sqrt{a^2 + \left(\frac{b}{p \sin^{3/2} \theta} \right)^2} , \qquad (2\text{-}20)$$

The constant a depends on the point resolution and geometrical stability of the detectors and the parameter b represents the resolution degradation due to multiple scattering, which varies with the incident particle momentum p and the track polar angle θ measured with respect to the beam direction. For the present vertex detector design for the TESLA experiment, the values of a and b are required similar for both projections, and take the values around for a and b of 4.2 μm and 4.0 μm, respectively.

2.2.6 Photon Interaction

2.2.6.1 Energy Loss by Photons

The physical process leading to photon detection is different than for heavy charged particles. The photon interaction with matters involves different physics processes, which contributions, thus cross sections vary with the energy of the photon. Incident photons may undergo the photoelectric absorption; the coherent scattering effect, the incoherent scattering effect or the interaction may result in the e^+e^- pair production. All these processes lead to partial or complete absorption of the photon energy. As a consequence of interactions, an incident photon either disappears or is scattered. Photon interaction coefficients, which give probabilities of each process to occur, for a wide energy spectrum are shown for silicon in Figure 2-4.

In photoelectric absorption, a photon disappears being absorbed by an atomic electron. The process results in ionisation by subsequent ejection of the electron from the atom. The energy of the liberated electron is the difference between the photon energy and the energy needed to extract the electron from the atom i.e. the binding energy of the electron. The recoil momentum is absorbed by the nucleus to which the ejected electron was bound. If the resulting photoelectron has sufficiently enough of kinetic energy, it may be a source of a secondary ionisation occurring along its trajectory, and in the case of the semiconductor material, it may create further e-h pairs. If the electron does not leave the detector the deposited energy corresponds to the energy possessed by the incident photon. This feature

of the photoelectric effect allows calibrating the gain of the detector chained with its read-out system if the energy required to create a single e-h pair is known.

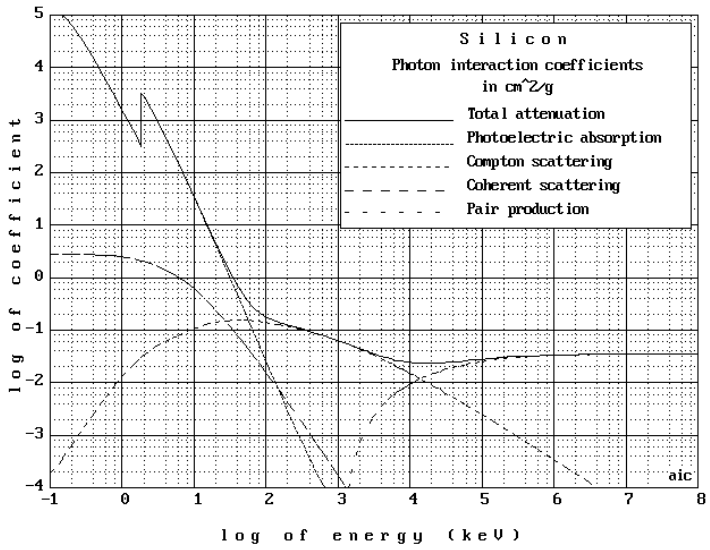


Figure 2-4: Photon interaction coefficients in silicon as a function of energy.

The clear image may be smeared by escape photons, which can leave the detector volume leading to less amount of energy deposited. These photons are actually the fluorescence photons emitted by deexciting atoms. Photons of fluorescence radiation are emitted by atoms after the ejection of a deep shell (K, L) electron. The incident photon creates a vacancy in the shell, thus leaving an atom in an excited state. Then, the vacancy can be filled by an outer orbital electron, giving rise to the emission of the characteristic X-rays photons of the fluorescence radiation. The missing energy, which is conveyed by the escape photons leads to, so called escape peaks in the measured energy spectrum as it is shown in Figure 2-5. Photon interaction coefficient for photoelectric absorption depends strongly on the atomic number of the absorbing material. The relevant cross section increases roughly as Z^3. For silicon, the photoelectric effect is a dominant process for photon energies below 100 keV.

The coherent and incoherent scattering effects are referenced as Rayleigh and Compton scattering, respectively. The Rayleigh scattering is characterised by the fact that no excess energy is transferred to the medium. The atoms are neither excited nor ionised and only the direction of the photon changes. The Compton effect consists of scattering of photons on free electrons. Essentially, the electrons are bound to atoms in matter. However, they can be

considered as effectively free if the photon energy is high with respect to the binding energy. The Compton effect leads to ionisation with the energy of the incident photon partially transferred to the free electron. The incident photon is deflected through an angle with respect to its original direction and its energy is changed.

The process of pair production involves the transformation of a photon into an electron/positron pair. In order to conserve momentum, this can only occur in the presence of a third body, which is usually a nucleus. In order to the pair production process may occur, the photon must have energy exceeding twice the rest-mass of an electron which is about 1.02 MeV.

2.2.6.2 Soft X-ray Photon Interaction in Silicon

Low-energy X-ray spectroscopy takes an important position in astrophysics and X-ray astronomy or for X-ray diffraction analysis in crystallography. Soft X-ray photons of energies below 10 keV are of the particular interest for testing gaseous and semiconductor detectors and integrated electronics used for their read-out in detector systems dedicated to particle detection in high energy physics experiment. The most widely used semiconductor material for fabricating of detectors as well as for microelectronic circuits is silicon.

Photons of energies below 10 keV interact dominantly through the photoelectric effect and the relevant absorption coefficients are relatively high providing good detection efficiency even in thin silicon detection volumes. Above the K-edge at 1.839 keV, there is about 92% probability of photon absorption by the K-shell electrons. The preferred relaxation process after ejection of the K-shell electron is radiationless (95.6%) via one of nine Auger electron groups. While, the Auger electrons are monoenergetic electrons produced by the absorption of characteristic (fluorescent) X-ray photons internally by the atom. The ejected electrons having an excess kinetic energy cause further ionisation creating on their way e-h pairs. The range R of the primary electron having the kinetic energy E_e is less than 1 μm, as given by equation (2-21) [21]. Thus the cloud of generated charge is confined close to the photon absorption point.

$$R\left[\mu m\right] = 40.8 \times 10^{-3} \left(E_e\left[keV\right]\right)^{1.5} \tag{2-21}$$

Photons of very low energies, below about 2 keV are ineffective for test purposes, since

they are absorbed by the surface layers of the detector or the glass coating of the integrated electronics chip. For a typical CMOS process, this may represent from 2 μm to 10 μm of material composed of metal paths (Al, Cu, Ti), oxide and passivation ($Si0_2$, Si_2N_3) on the top of the active volume. The amount of charge resulting from the photon absorption can be determined knowing the energy required to create an e-h pair. If the development of the charge cloud of secondary electrons is assumed to take place in field-free region, so that there is no increase in electron energy between collisions thus there is no charge amplification, the total amount of dislodged carriers can be calculated as a ratio of the absorbed photon energy and the mean energy for one e-h pair creation W. The intrinsic FWHM energy resolution of the detector, in the case of the full energy absorption of the photon energy E, is given by the following expression

$$R = 2.35\sqrt{\frac{F\,W}{E}}, \tag{2-22}$$

where F is known as the Fano factor. The Fano factor gives estimation of fluctuations of the signal charge in the detector. This coefficient describes a statistical distribution of the number of ionised pairs being produced if a well-defined energy is lost in the medium. Since two types of interactions are possible, i.e. these leading to formation of a mobile charge and those resulting in lattice excitation, it can be assumed that in course of energy deposition, it occurs N_x excitations and N_i ionisations. The sum of energies going into lattice excitations and ionisation is equal to the total energy E deposited by the incident particle. Assuming gaussian statistics the variances in the number of excitations and ionisations are $\sigma_x = \sqrt{N_x}$ and $\sigma_i = \sqrt{N_i}$, respectively. For a given energy deposited in the sample, a fluctuation in excitations must be balanced by an equivalent fluctuation in ionisation, which yields: $W_i\sigma_i = W_x\sigma_x$, where W_i and W_x are the energies required for single ionisation and excitation, respectively. Since, each ionisation leads to a charge pair that contributes to the signal $N_i = E/W$, where W is the average energy loss required to produce a charge pair. Thus, after some rearrangements, the variance in the number of ionisations can be written by:

$$\sigma_i = \sqrt{E/W}\cdot\sqrt{W_x/W_i\left(W/W_i - 1\right)}. \tag{2-23}$$

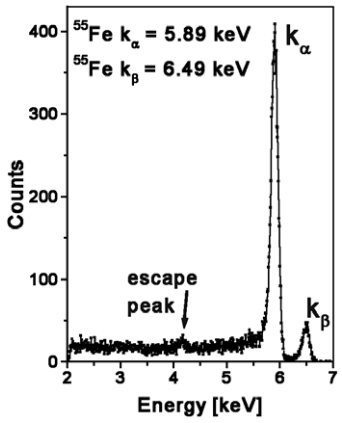
The second factor under square root is called the Fano factor F, and the variance in signal

charge can finally be written as: $\sigma_i = \sqrt{N_i F}$. For ionising detector F is typically around 0.2 - 0.3 for gases, whereas for solids like silicon it is in the area of 0.12 - 0.16. Both W and F coefficients are considered as material properties. It has been observed that the W factor is an increasing function of X-ray energy below 0.5 keV [20]. Its characteristic exhibits some irregularities as a function of the photon energy close to each absorption edge. The W value depends weakly on the temperature reflecting the temperature dependence of the silicon band gap.

Processes leading to production of e-h pairs in the silicon detector material are valence band ionisation, plasmons excitations and core-shell ionisations. Each of these processes leads to ionisation but requires different energy for an e-h generation. Actually, the W factor includes all reactions, also those, which do not lead to ionisation, e.g. example electron-phonon interactions. This gives rise to the higher value of the mean energy for an e-h pair production than energy band gap. The measured value of the energy W equals to 3.658 eV for a single e-h pair created at 170 K [20]. The temperature dependence of W is given by the temperature coefficient dW/dT which value was determined to be about 0.1 $\%K^{-1}$. This results in W =3.645 eV for a single e-h pair created at room temperature. The measurement of the Fano factor for silicon reported the value about 0.155 [20], which is also slightly dependent on the temperature. The Fano factor is determined less accurately than the energy W.

The Monolithic Active Pixel Sensors (MAPS) detectors, which are described in the following parts of this work, were extensively tested using a ^{55}Fe source. The iron source is universally used in testing of CCDs especially in X-ray astronomy and other detectors where it is mainly used for calibration purposes. This source delivers photons from two dominating γ emission modes i.e. Mn K_α 5.9 keV and Mn K_β 6.49 keV photons. The yield of 6.49 keV photons from the second emission mode is only 12% of the number of 5.9 keV photons from the first mode. The photons have absorptions lengths of 26.95 μm and 35.35 μm, respectively. Figure 2-5 shows a photon spectrum of a ^{55}Fe source measured with the DEPFET device, whose description is given in Chapter 3.3.4, at room temperature, and gives the characteristic of the photons emitted by this source and of the related e-h pairs creation coefficients for silicon. The relatively large value of the absorption length close to 30 μm allows photons to penetrate the whole active volume of the tested device. In the case of the

discussed MAPS devices, the active volume of the detector is limited to the epitaxial layer of the thicknesses between 2 μm and 15 μm. Thus, the signals due to X-ray photons from an iron source could originate from the whole depth of the active volume.



a)

parameter	value
emission ^{55}Fe @ 5.90 keV	24.4%
emission ^{55}Fe @ 6.49 keV	2.86%
half value layer (HVL) @ 5.90 keV in Si	18.68 [μm]
half value layer (HVL) @ 6.49 keV in Si	24.50 [μm]
average energy/electron-hole pair (W) @ 170K, 5.9 keV in Si	3.658* eV –0.01%K^{-1}
Fano factor (F) @ 170K, 5.9 keV in Si	0.155*

* G.W.Fraser, Nucl. Instr. and Meth. A 350 (1994) 368 b)

Figure 2-5: (a) Spectrum of the photons emitted by a ^{55}Fe source measured with the DEPFET device at room temperature, (b) characteristic of the emitted photons from the iron source and e-h pairs creation coefficients for silicon.

2.3 Radiation Damage

Radiation hardness is required for many particle detectors and the read-out electronics in current and future particle physics experiments. The very high reaction rate and also beam induced background in these experiments put stringent requirements on the radiation hardness of the basic detector components. This is particularly true for all tracking devices and their electronics, because of their location close to the beam line and the interaction point. Also, possible applications in space require hardened devices. The tracking devices are exposed to large fluences of damaging radiation and have to retain a minimum SNR for efficient particle detection.

In semiconductor devices, incident particles produce three main types of effects: atom displacements from their sites in the lattice, transient ionisation and long term ionisation in insulators inducing regions of fixed charge carriers and formation of interface defects*. The first type of effects usually starts at lower doses to be more destructive for detecting devices

* The most strict requirements for radiation hard detectors and electronics in high energy physics applications refers to the LHC machine. The CMS experiment is characterised by the fluence of 10^{15} hadrons/cm^2 and the total dose of 35 Mrad at the vertex tracker area closest to the beam over 10 years of the experiment operation.

than for the read-out electronics. The displacement process affects the properties of the bulk semiconductor and it is known as *bulk damage*. The formation of radiation induced trapped charges and interface defects are referred under the term *surface damage*. Ionising radiation is mostly responsible for deteriorating performances of the read-out electronics.

On a macroscopic scale, damage in solid state detectors causes, an increase of a leakage current translating into an increase in noise and a reduction in the amount of collected charge due to the charge carrier trapping mechanism, the decrease of the carrier's mobility and their lifetime [22, 23]. Therefore, the SNR decreases with progressing radiation damage. As far as read-out electronics is concerned, it was found that the degradation of the parameters of bipolar and MOS devices is caused by radiation induced surface effects at the Si-SiO_2 interface, as well as by defects in the bulk.

2.3.1 Displacement Damage

Excessive radiation by massive particles e.g. neutrons, protons, pions and in some extent electrons or by high energy photons may induce defects which are referred to atom displacements in the crystal lattice of the detector material. These are dislocations of atoms from their normal sites in the lattice resulting in less ordered structures. The transferred energy is expressed as non-ionising energy loss (NIEL) for incident particles. The NIEL value is usually scaled by referring to the equivalent fluence of 1 MeV neutrons producing the same damage as an examined beam of the fluence Φ with a given spectral energy distribution [24]. The crystal defects may be referred to as point defects for local single-atom displacements or cluster defects characterised by large regions of crystal lattice disturbances. Isolated displacements are created mostly by electromagnetic radiation of low energy electrons and X-ray photons, that can deliver only small energy to the recoil Si atom creating single vacancy-interstitials pairs*. The massive particles create rather cascades of secondary knock-on atoms [25] by knocking out Si atoms having sufficient energy to further displace atoms in the crystal. At the first step, the primary particle hits an atom in the lattice transferring enough energy to displace it and creating primary interstitials and vacancies. If the displaced atom possesses high kinetic energy, it can knock out additional atoms. The

* The vacancies are referred as empty lattice sites and interstitial atoms are those which are knocked out of their normal positions in the crystal lattice.

generated groups of interstitials and vacancies can recombine and repair the initial defects, or the primary defects rearrange, migrate, interact with impurities and finally form usually irreversible defect complexes, which remain as permanent radiation damage. Vacancies create active defect complexes by interaction with the impurities such as oxygen, carbon, atoms of dopants, or with themselves and form traps in the silicon band gap, which capture and emit charge carriers. When irradiated samples are heated, thermally activated motions increase rearrangements of the lattice defects, which may result in restoration of the ordered crystal structure. The practical obstacle for this annealing operation is a high temperature required, which could be destructive for the device. Figure 2-6 gives an example of the development of cluster damage due to a primary knock-on silicon atom of 50 keV. In the inset of this figure, the model of an atomic displacement due to electromagnetic radiation and the impact of a heavy particle creating a cascade of secondary knock-on atoms is illustrated. The mean free path between two successive collisions decreases towards the end of the recoil particle range, resulting in terminal cluster damages. Defect clusters have high local defect density and can be tens of nanometers wide. They have more critical effect on the properties of semiconductor devices than point defects

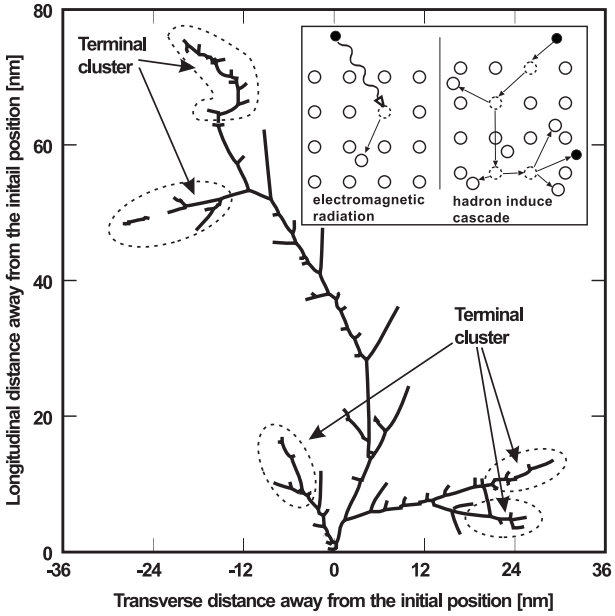


Figure 2-6: Development of cluster damage and model of atomic displacement (right upper corner) due to electromagnetic radiation and impact of the heavy particle.

Additionally, in the case of high energies, nuclear reaction can occur, producing several fragments or secondary particles. The fragments produced in the nuclear reaction may migrate through the lattice causing further displacements if they have sufficient energy.

The electrical properties of a semiconductor device are affected by the concentration of point defects. Point defects introduce energy levels in the band gap. These energy levels can act as acceptors, donors or charge traps and modify the lifetime of charge carriers. The carrier lifetime is related to the concentration of defects N_{def} by

$$\tau_{def} = \frac{1}{v_{th}\sigma_{def}N_{def}}, \tag{2-24}$$

where v_{th} is the thermal velocity* of charge carriers, and σ_{def} is the charge carrier capture cross section of the point defect. The production rate of point defects and cluster defects in the irradiated material depends both on the cross section for the interaction and the intensity of the incident radiation. The cross section depends on the particle type and on the energy spectrum [26]. The estimate for the formation of a vacancy-interstitial point defect is 25 eV in silicon. The energy threshold for electrons to displace a Si atom is around 260 keV, and electrons need more than 5 MeV to produce clusters [27], whereas only 190 eV is required for a neutron to do the same effect and it needs only about 15 keV to create clusters [28]. A recoil Si atom needs about 5 keV of energy to displace other Si atoms in the crystal. Since these displacements are closely situated, most of them repair and only 2% of all generated defects form electrically active states.

In a very simplified picture the damage effects can be considered to be proportional to the fluence Φ of the particle beam generating the damage. The carrier lifetime after irradiation is decreased due to various mechanisms leading to carrier recombination. However, independent processes can be combined and described by a single lifetime τ_R, which can be calculated by Matthiessen-like† summing rule. If the carrier had an initial lifetime before irradiation τ_0 the dependence of the lifetime on the irradiation fluence is

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* Under thermal equilibrium, the average energy of a conduction electron is obtained from the theorem for equipartition of energy: $\frac{1}{2}kT$ units of energy per degree of freedom. Since, the electrons in a semiconductor have three degrees of freedom, the kinetic energy of the electrons is given by $\frac{1}{2}m_e v_{th}^2 = \frac{3}{2}kT$, where m_e is the effective mass of electrons and V_{th} is the average thermal velocity.

† Original Matthiessen summing rule refers to the resistivity of the metallic crystal materials. It claims that the resistivity of a metallic crystal is composed of two additive parts: the resistivity due to crystal imperfections and the resistivity due to thermal agitation of the metallic ions.

given by

$$\frac{1}{\tau_R} = \frac{1}{\tau_0} + \frac{1}{\tau_{def}} = \frac{1}{\tau_0} + \kappa_\tau \Phi , \tag{2-25}$$

where κ_τ is the carrier lifetime damage constant. For large fluences, the factor $\kappa_\tau \Phi$ starts to dominate in equation and the carrier lifetime becomes inversely proportional to the irradiation dose. It decreases linearly like $(\kappa_\tau)^{-1}$.

The displacement effects manifest in the increase of capture, generation, and recombination rates of the non-equilibrium charge carriers. In detectors made of high quality, low doped ($\sim 10^{12}$ cm^{-3}), they cause changes of the internal electric field, due to the modified effective doping concentration. This may go even up to the inversion of the conduction type at very high irradiation doses. Other effects are the increase of the leakage current, charge collection losses, changes in capacitance and material resistivity. Increase of the bulk dark current is mostly due to defects situated near the midgap level. Irradiation with heavy particles often creates large non-uniformities in the dark current spatial distribution in the detector. In the case of pixel detectors, cells with much higher dark current than the average dark current are called *hot pixels*. Dark current is an issue only for near-room temperature operation or long integration times, because it can be reduced to negligible values by cooling. The losses in the collected charge are caused by trapping by bulk defects. The trapping is due to the different time constants and temperature dependence of the electron capture and emission processes [29]. The mechanism of charge losses issues from capturing and later releasing of some charge carriers from signal packets by traps. Those electrons, which are released after the time required for one full read-out of the detector do not join their original signal packet and account for collection charge losses*. The capture time constant is usually of the order of several hundreds nanoseconds, while the emission time constant is temperature dependent and varies from seconds to microseconds as the temperature increases. At high temperature, traps are occupied only for a short time. Thus trapped electrons originating from ionisation are able to join their signal packet for read-out, since they are emitted in a short time following trapping. On the other hand, the emission

* In the case of CCDs, trapping mechanism due to bulk defects accounts for charge transfer inefficiency. When the signal charge packet being transferred encounters traps some of its electrons are captured and later released. Those electrons, which are released behind do not join their original packet and the charge packet is smeared which is interpreted as the charge transfer inefficiency.

time constant at low temperature of the defects can be very large and traps which are filled with electrons, remain occupied for a time much longer than the time of charge accumulation within the pixel area e.g. for practically used charge integration time. Therefore, the defects cannot capture signal electrons and thus, charge losses due to carrier trapping are insignificant at high and low temperature. At temperatures between these two extremes there is a maximum in charge losses.

The most widely used technique for study of radiation induced bulk defects is the Deep Level Transient Spectroscopy (DLTS) [30]. DLTS is used to measure the energy levels, capture cross sections and concentrations of defects.

2.3.2 Ionisation Damage

Radiation damage may also be induced by direct ionisation due to charged particles and photons of sufficient energy to produce e-h pairs in the medium. The ravages of ionising doses due to incident charged particles and photons are concentrated at interfaces between different materials, e.g. at the Si-SiO_2 interface. Ionisation takes place in silicon dioxide, while about 18 eV of deposited energy is required for the creation of one e-h pair. The charge is generated along tracks of charged particles, or close to conversion points of incident photons, or in restricted regions around nuclear reactions. The ionisation damage consists in trapped charges inside insulators e.g. silicon dioxide and at interfaces between insulators and semiconductor materials and ruptured chemical bonds at these interfaces. Many of the e-h pairs produced manage to recombine in the initial phase and do not cause any negative effect. The others carriers, which did not recombine, diffuse or drift away from the point where they were created. A number of charge carriers get blocked in some parts of the device, giving rise to the presence of zones of the space charge. The effects due to charged regions do not alter the crystal lattice and are usually reversible. At any Si-SiO_2 interface there are numerous interface traps, which result from the strained or dangling silicon bonds at the boundary between the two materials. The density of the interface traps depends strongly on the processing parameters, such as oxidation temperature, and is usually in the range from 10^9 cm^{-2} to 10^{10} cm^{-2}. Ionising radiation causes the density of these traps to increase and modifies their energy distribution, giving rise to radiation induced interface traps, hence new energy levels are introduced in the band gap at the Si-SiO_2 interface. These interface states

are occupied by electrons or holes, depending on the position of the Fermi energy level at the interface. They play the role of additional acceptor or donor states, which under thermal equilibrium are charged. According to experiments, most of the traps with energy levels situated in the upper half of the band gap are acceptors and traps below the midgap are donors [31]. Trapped charges alter the electrical characteristics of the devices by modifying the electric fields inside. The energy levels close to the midgap may act as trapping centres for charge carriers generated by incident particles in the detector. This effect is observed as partial charge collection after irradiation. The charge carriers generated by an incident particle are blocked in trapping centres and are being released with some delay after the particle passage. The increased density of energy states in the band gap, which can act also as generation-recombination centres, increases the recombination velocity at interfaces. This effect translates primarily into an increased leakage current. For some detectors, the generation at the Si-SiO_2 interface is the dominant source of a dark current.

Ionisation damage is of the main concern for the front-end electronics. Read-out circuits suffer from the effect of positive charge build-up, the decreased carrier's surface mobility and the high density of interface states with energy levels in the band gap [32]. Due to the creation of new interface traps, both NMOS and PMOS transistors, suffer from the increase of absolute value of their threshold voltages* [33]. Interface traps are generated in at least two stages [34] as a prompt and delayed component. The prompt component is connected with direct interaction of radiation with the interface. The responsibility for the delayed component is assigned to atoms of hydrogen, which are present in the oxide due to the fabrication methods of integrated circuits. In the ionisation process, the hydrogen atoms are stripped out of electrons. The produced positive ions are attracted towards the lowest electric potential, which is at the interface between the oxide and the bulk silicon and between the gate made of poly-crystalline silicon material and the oxide in the case of an NMOS transistor and a PMOS transistor, correspondingly. NMOS transistors are particularly sensitive to the formation of interface states in the closest vicinity of the conduction channel. This is due to polarisation of NMOS transistors with positive voltage on the gate. The increased density of the interface states has also an impact on flicker noise of the

* Threshold voltage in the case of a MOS transistor is defined as the minimum voltage between a transistor gate and a source to initiate conduction of a drain current.

NMOS transistor which level is significantly higher compared to the PMOS device, and is further deteriorated after irradiation.

The amount of the trapped charge carriers in the oxide is proportional to the number of defects. For this reason, the control of the gate oxide quality is essential for the radiation-hardened technologies*. The charge trapping mechanism in the oxide volume concerns merely the positive charge carriers i.e. the holes, because of the high difference in the hole and electron mobilities [35] and the increased capture cross section for holes close to the interface boundaries. The typical mobility in SiO_2 for electrons at room temperature is ~20 $cm^2V^{-1}s^{-1}$ and increases to ~40 $cm^2V^{-1}s^{-1}$ at temperature below 150 K. Hole mobility usually varies from 10^{-4} $cm^2V^{-1}s^{-1}$ to 10^{-11} $cm^2V^{-1}s^{-1}$ as a function of temperature and electric field. Because it is many orders of magnitude lower than the electron mobility, hole transport through the oxide takes place in the time scale of seconds to hours. Low hole mobility blocks holes in the oxide, whereas electrons can leave the oxide in a short time following irradiation. Figure 2-7 shows a mechanism of the positive charge trapping in the oxide underneath an NMOS transistor gate.

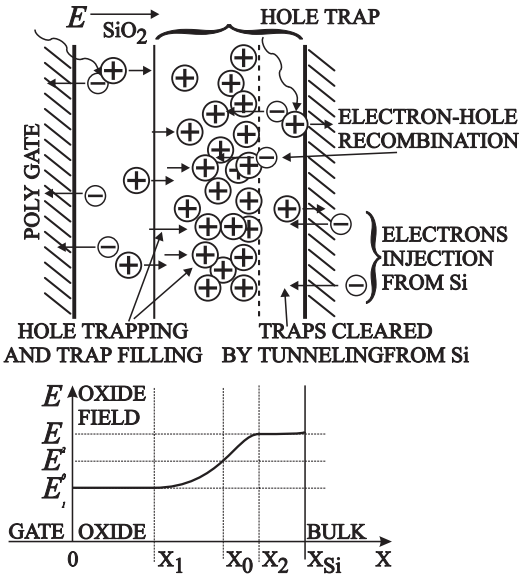

Figure 2-7: Positive charge trapping process in the oxide underneath the MOS transistor gate as a result of ionising irradiation.

The electrons from created e-h pairs rapidly escape from the oxide region. Their movement

* In oxides, designed as "hard", the trapping factor can be as low as 0.01, while in "soft" oxides this ratio can be close to 1.

is caused by the presence of the high electric field in these regions. In contrast to electrons, some of the holes moving towards the negative electrode get stuck within several nanometers from the SiO_2-Si interface. In the case of the PMOS transistor, where the bias voltage has the reverse polarisation with respect to the NMOS device, the holes are grouped close to the SiO_2-gate interface. Some part of the stuck holes, i.e. those that are closest to the interface, may recombine with electrons mounting from silicon. The electrons reach the oxide volume by the tunnel effect [36] and the effect is referred to as a tunnel-effect based recovery, which reduces the amount of positive charge trapped in the oxide. The probability of tunnelling electron jump increases exponentially with decreasing thickness of the concerned oxide volume. Thus, the thin oxide of a deep sub-micrometer MOS transistor is intrinsically more radiation tolerant than thicker oxides used in past technologies. For gate oxide thicknesses above approximately 20 nm, the shift of threshold voltage after irradiation ΔV_{th} is proportional to the squared value of the oxide thickness $\Delta V_{th} \propto t_{ox}^2$ [*]. On the other hand, the threshold voltage shift below 20 nm decreases even faster approaching the dependence $\Delta V_{th} \propto t_{ox}^3$ at the corresponding irradiation dose [37]. In the case of thin oxides, the similar dependence is observed for the density of the interface states [35]. Thus, for processes used nowadays for integrated circuits fabrication, the threshold voltage shift and the increase in the interface state density are very small. Modern chips are able to withstand doses of several tens of Mrad (1 rad=0.01 Gy). However, if the trapped charge density close to the interface is high enough to yield an inversion layer in the underneath semiconductor material, conduction paths between different components fabricated on the same substrate may be induced. Standard bulk CMOS processes use p-type substrate wafers, and accumulated positive charges may provoke short circuits in the design. The effect is strongly enhanced under thick oxide regions, where leakage currents appear close to the interface. Shallow surface channels can be created between different n-type regions implanted on the chip if they are separated only by lightly doped p-type silicon. Moreover, the charge accumulated at the ends of polysilicon gates of designed in a classical rectangular form NMOS transistors may prevent them to be switched off completely. This is why, the use of enclosed NMOS

[*] Assumed uniform generation of e-h pairs in the oxide by radiation the threshold voltage shift is given by $\Delta V_{th} = -\frac{q}{\varepsilon_{SiO_2}} K_g f_y D f_T t_{ox}^2$, where K_g is the charge generation coefficient, f_y is the free charge yield, D is the radiation dose, f_T is the fraction of radiation induced holes that are trapped in the oxide, t_{ox} is the oxide thickness.

transistor gates and p^+-type guard-rings of increased doping were introduced for a wide use. Complying with this design rule makes radiation hard electronics possible using standard inherently radiation-soft processes [38]. This is commonly used now for radiation hardened read-out circuits designed for the high energy physics experiments. Figure 2-8 shows the principle of the radiation tolerant layout of an NMOS transistor with enclosed polysilicon gate and the use of a p^+-type guard-ring protecting against leakage currents between n-type regions in the design.

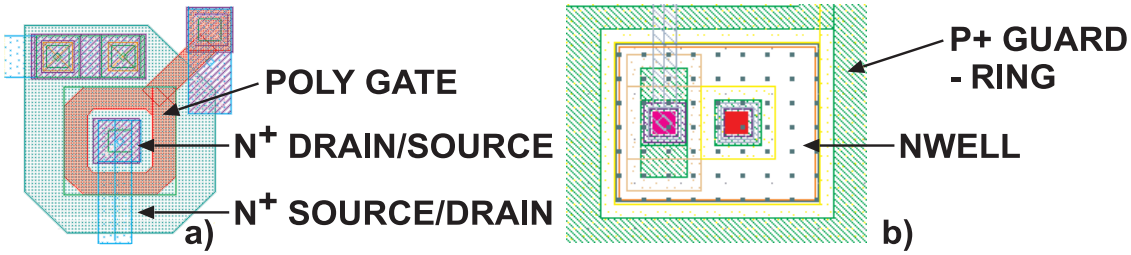

Figure 2-8: (a) Radiation tolerant layout of an NMOS transistor with enclosed polysilicon gate in CMOS process (p^+ guard-ring is not shown), (b) layout of an n-well/p-sub diode with p^+-type guard-ring protecting against leakage currents.

Chapter 3

POSITION SENSITIVE DETECTORS BASED ON SEMICONDUCTOR

3.1 Introduction

Tracking and vertex detectors consist of several layers combined in segments of one- or two-dimensional detectors placed around the interaction point. The impact position of a particle is obtained by processing electrical signals from the detector. In the case of highly segmented detecting elements, the information on spatial position of hits comes out directly analysing magnitudes of individual signals as a function of their positions in the acquired data. On the other hand, exploiting undivided detectors, some appropriate processing is needed, e.g. consisting in deconvolving the spatial information from time properties of registered signals. Traditionally, microstrip silicon sensors are used, characterised by fast response and simplicity of the read-out architecture. The drawback of microstrip detectors is their inability of solving multi-track ambiguities. In some applications, demanding two-dimensional but only slow read-out at low event rate tracking, silicon drift chambers are used. Consecutively, highly segmented pixel detectors emerged for particle tracking serving an important role for the first time in the DELPHI experiment. Pixel detectors offer high system integration and the capability of dealing with high particle densities. The continuous development of pixel detectors is aiming at optimisation of their performances to match particular requirements of given experiment. The optimisation includes improvements in: spatial resolution, capability of solving multi-track and very close track ambiguities, radiation hardness, read-out speed and reduced multiple scattering.

Signals in semiconductor detectors originate in the collection of charge carriers generated by impinging charged particles in the active volume of the detector. The active detector volume has usually the form of a fully depleted reverse biased diode with charge collection achieved through carriers drifting in an electric field. The movement of charge carriers induces currents passing through the detector electrodes and the resulting signals are processed by the front-end electronics. Classically, the read-out electronics is fabricated as a separate chip, which is wire or bump bonded to the strip or pixel detector, respectively. One

of the main issues for pixel detectors is to integrate the detector and the read-out electronics onto the same substrate. This approach yields a monolithic, thus thin and compact particle detector. Up to now several ideas were already proposed and verified on the prototyping stage. In spite of promising results, all of these efforts were requiring dedicated fabrication processes, and were not introduced in any practical application. Observing, that an efficient charge collection can be achieved through thermal diffusion from a thin and only partially depleted epitaxial layers, a new kind of monolithic pixel sensors was proposed. This type of detectors i.e. Monolithic Active Pixels Sensors, beside of Charge Coupled-Devices already successfully used in the SLD* experiment, are considered as a viable candidates for a future linear collider vertex detector.

3.2 Signal Formation and Noise in Semiconductor Detectors and Electronics

3.2.1 Charge Collection

Semiconductor detector work in principle like ionisation chambers. The positive and negative charge carriers, i.e. electrons and holes, created by radiation are being separated and by an electric field across the detection volume. The detector electrodes inducing currents in the external circuit collect these mobile charges. The currents are sensed and processed by the front-end electronics and are used to measure energy or position. A high field in the detection volume is desirable since it allows fast detector response and improves charge collection efficiency due to reduced charge trapping and guided charge motion. In some detector technologies, high electric fields cannot be employed because of the limited voltage range allowed by the fabrication process. In these cases, the charge collection is achieved partially through thermal diffusion, and the electric field exerts force on the charge carriers only close to the collecting electrodes. The desired high SNR for a detector is obtained by a high charge yield and small continuous leakage current, significantly lower than the currents induced by generated charges.

Semiconductor materials are characterised by a moderate band gap, thus semiconductor detectors provide a large number of charges. The conduction band is only empty at 0 K. As

* SLD stands for Stanford Linear Accelerator Collider (SLAC) Large Detector.

the temperature is increased, thermal excitations promote electrons across the band gap into the conduction band. Silicon, which is the most commonly used material for detector fabrication, in pure form, has a resistivity of approximately 400 $k\Omega \cdot cm$ at 300 K*. In reality, crystal imperfections and minute impurity concentrations decrease the resistivity by at least one order of magnitude with respect to the intrinsic material. Thus, high-field region with low DC current in semiconductor is mostly achieved by the depletion region of a p-n junction [39].

Figure 3-1a shows a reverse biased p-n junction, which can be considered as a parallel plate detector. A lightly doped n-type bulk is used as an active detector volume. The applied reverse bias is lower than the voltage needed to fully deplete the detector volume and the diode is undepleted. The expression of the electric field, shown in Figure 3-1b, inside the bulk is

$$E(x) = \begin{cases} E(x) = -\dfrac{qN_D}{\varepsilon_{Si}}(x - W) = E_0(W - x) & \text{for} \quad x \le W \\ 0 & \text{for} \quad x > W \end{cases}, \tag{3-1}$$

where N_D is the concentration of donor impurities in the bulk and W is the depletion depth which under reverse bias V_b is approximately given by

$$W \approx \sqrt{\frac{2\varepsilon_{Si}(V_{bi} - V_b)}{qN_D}} \quad \text{for} \quad V_{bi} = \frac{kT}{q}\ln\frac{N_A N_D}{n_i^2}, \tag{3-2}$$

which is the total electrostatic potential difference between the p-side and the n-side neutral regions at thermal equilibrium, called the built-in potential. The N_A parameter is concentration of acceptor impurities at the p-side of the junction, and n_i is a carrier concentration intrinsic to an ideal crystal where the only population mechanism is excitation across the band gap. The product of the electron and hole concentrations $np = n_i^2$ expresses the law of mass action. It requires only that the Boltzmann approximation holds, so it is not limited to undoped or ideal crystal. The field drops linearly from its maximum value at the junction to zero at the opposite contact. The electric field lines are normal to the diode

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* Resistivity of a semiconductor material is defined as $\rho = 1/q(n\mu_n + p\mu_p)$, where n and p are concentrations, and μ_n and μ_p are mobilities of electrons and holes, respectively. For intrinsic semiconductor material $n = 2(2\pi m_e kT/h^2)^{3/2}\exp(-(E_C - E_F)/kT)$ and $p = 2(2\pi m_h kT/h^2)^{3/2}\exp(-(E_F - E_V)/kT)$, where m_e and m_h are effective masses of the electron and the hole, and E_C, E_V and E_F are conduction, valence and Fermi energy levels, respectively.

surface and are directed from the anode, which is the n^+-metal ohmic contact towards the cathode – the p^+ contact. The detector bulk is completely depleted of mobile charges when W=d. This occurs at the externally applied depletion voltage

$$V_d = \frac{qN_D W^2}{2\varepsilon_{Si}} - V_{bi}, \tag{3-3}$$

When the bias voltage is still increased, a uniform field due to the voltage beyond depletion is added yielding

$$E(x) = \frac{2(V_d + V_{bi})}{W}\left(1 - \frac{x}{W}\right) + \frac{V_b - V_d - V_{bi}}{W} = E_0'\left(1 - \frac{x}{W}\right) + E_1'. \tag{3-4}$$

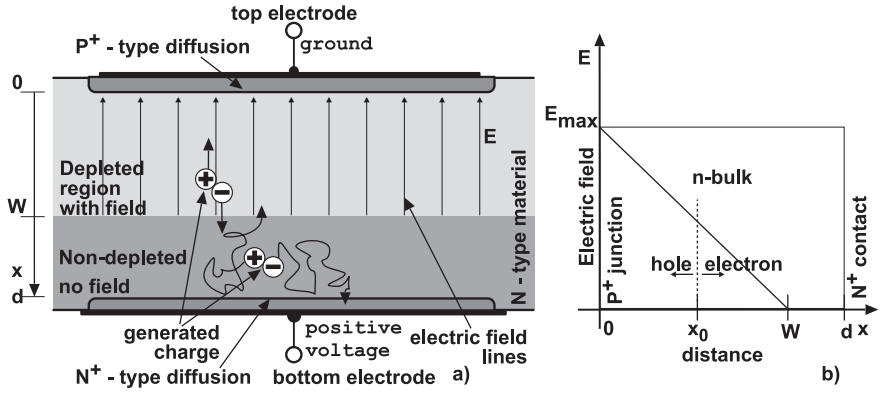

Figure 3-1: (a) Movement of charge carriers contributing to the detector signal, (b) electric field distribution in the silicon diode.

For the detectors operated at partial depletion, the charge carriers generated in the not depleted region may contribute to the total signal if only they reach the depletion zone. Otherwise they are lost due to recombination or they may diffuse reaching a far part of the detector. The local velocity of a charge carrier is given by

$$v(x) = \mu E(x) = \mu E_0 (W - x), \tag{3-5}$$

The carrier velocity is a function of the electric field, at every position. In silicon, at 300 K the mobility at low fields is 1350 cm^2/Vs for electrons and 480 cm^2/Vs for holes. The mobility is constant for electric field up to about 10 kV/cm, but then an increased phonon emission reduces the energy imparted into kinetic energy of charge carriers. Thus the mobility decreases. At high fields above 100 kV/cm, the carriers attain a constant* drift

* At high field above 100 kV/cm, the mobility $\mu \propto 1/E$.

velocity of 10^7 cm/s. The time required for charge carriers (holes) originating at x_0 to reach a point x is

$$t(x) = \int_{x_0}^{x} \frac{1}{v(x)} dx = \frac{\varepsilon_{Si}}{\mu_p \, q \, N_D} \ln \frac{W - x}{W - x_0}. \tag{3-6}$$

Thus, the time required for holes originating in a given point x_0 to reach the cathode is expressed by

$$t_{x_0} = \tau_{coll,p} \ln \frac{W}{W - x_0}, \quad \text{where} \quad \tau_{coll,p} = \frac{\varepsilon_{Si}}{\mu_p q N_D}. \tag{3-7}$$

For the electrons drifting towards the low-field electrode at x=W, equation (3-7) diverges, since the electron velocity close to the boundary of the depletion zone approaches 0. However, it can be rewritten giving the position as a function of time

$$x(t) = W - (W - x_0) e^{-\frac{t}{\tau_{coll,n}}}, \quad \text{where} \quad \tau_{coll,n} = \frac{\varepsilon_{Si}}{\mu_n q N_D}. \tag{3-8}$$

According to this simply consideration, a charge drifting towards the low field region is never collected (in reality this is a achieved by diffusion), although after a time $t = 3\tau_{coll,n}$ the carriers traverse 95% of the detector. The collection time constants $\tau_{coll,n}$ and $\tau_{coll,p}$ are independent of the applied voltage, but determined only by the doping concentration of the bulk material and the carrier mobility. In a typical n-type silicon of 10 $k\Omega\,cm$ resistivity, $\tau_{coll,n} = 10.5$ ns and $\tau_{coll,p} = 31.5$ ns.

The collection time is significantly reduced when the detector is operated at bias voltages exceeding the depletion voltage V_d. In this case, equation (3-4) the time required for a charge carriers originating at x_0 to reach a point x is

$$t(x) = \frac{W}{\mu E_0'} \ln \frac{E_0' + E_1' - E_0' \frac{x}{W}}{E_0' + E_1' - E_0' \frac{x_0}{W}}, \tag{3-9}$$

which yields collection times

$$t_{coll,p} = \frac{W}{\mu_p E_0'} \ln\left(1 + \frac{E_0'}{E_1'}\right) \quad \text{and} \quad t_{coll,n} = \frac{W}{\mu_n E_0'} \ln\left(1 + \frac{E_0'}{E_1'}\right), \tag{3-10}$$

for holes and electrons traversing the whole detector thickness, respectively. The collection times for holes and electrons are considerably less than in the partially depleted device. For n-

type silicon of 10 kΩcm resistivity, a detector thickness of 300 μm, and a reverse bias voltage V_b=60 V = $2V_d$ the collection times are 12 ns and 36 ns for electrons and holes, respectively.

3.2.2 Signal Formation in Semiconductor Detectors

The movement of the generated charge induces a signal on the detector electrodes. The height of the generated signal depends on the distance of the charge carrier from the electrode. For the simple situation of a detector with plane plates at fixed potential, as it is depicted in Figure 3-1, the induced charge on the plate may be calculated using the image charge method [40].

Assuming the presence only of the top plate in Figure 3-1 and fully depleted operation of a detector, a single charge q, fixed at the position x_0 below a conductive plate, has its image charge of the opposite sign in the same distance x_0 on the opposite side of the plate. A superposition of charge pairs of opposite sign placed symmetrically on two sides of a plane results in a field that is normal to the plane. This approach allows to satisfy the boundary conditions imposed on the electric field on the conductor surface. The potential due two point charges of equal magnitude spaced a distance $2x_0$ apart is expressed in the cylindrical co-ordinates (r, φ, x) according to the formula

$$\Phi = \frac{q}{4\pi\varepsilon_{Si}}\left(\frac{1}{\sqrt{r^2+(x_0-x)^2}}-\frac{1}{\sqrt{r^2+(x_0+x)^2}}\right), \tag{3-11}$$

where in the symmetry plane, the normal components add, while the tangential components cancel. Differentiating of equation (3-11) allows to determine the surface charge on the plate, which after evaluation is given by

$$\sigma_s = \varepsilon_{Si}\,E\big|_{x=0} = -\varepsilon_{Si}\left.\frac{\partial\Phi}{\partial x}\right|_{x=0} = -q\frac{x_0}{2\pi\left(r^2+x_0^2\right)^{3/2}}. \tag{3-12}$$

In order to have equations (3-11) and (3-12) and others in this paragraph valid, the dielectric constant is assumed to be equal on both sides of the plate, which does not influence the generality of the result. The induced charge density is a function of the radial co-ordinate r and the position x_0 of the original charge. When the circular surface region, with radius rad and centred around the axis between the fixed charge and its image charge, is chosen for the

top electrode, the induced charge on it is determined by

$$q_{ind}^{top,single} = \int_0^{2\pi} d\varphi \int_0^{rad} \sigma_s r\, dr = -q\left(1 - \frac{x_0}{\sqrt{rad^2 + x_0^2}}\right). \tag{3-13}$$

It can be noticed that the induced charge on the top electrode approaches –q in the limit of large electrode radius. In order to include the effect of the bottom plate of the detector into considerations, the method of multiple image charges must be used. Its application is illustrated in Figure 3-2a. All image charges lie on one axis and their potentials can be superimposed. The resulting potential is expressed as an infinite sum, where each sum constituent is obtained by applying equation (3-13). Thus, the total induced charge on the top plate, resulting from integration over a surface region with radius rad, is calculated by

$$q_{ind}^{top,two} = q\left(\sum_{k=1}^{\infty}\left(1 - \frac{2kd - x_0}{\sqrt{rad^2 + (2kd - x_0)^2}}\right) - \sum_{k=0}^{\infty}\left(1 - \frac{2kd + x_0}{\sqrt{rad^2 + (2kd + x_0)^2}}\right)\right). \tag{3-14}$$

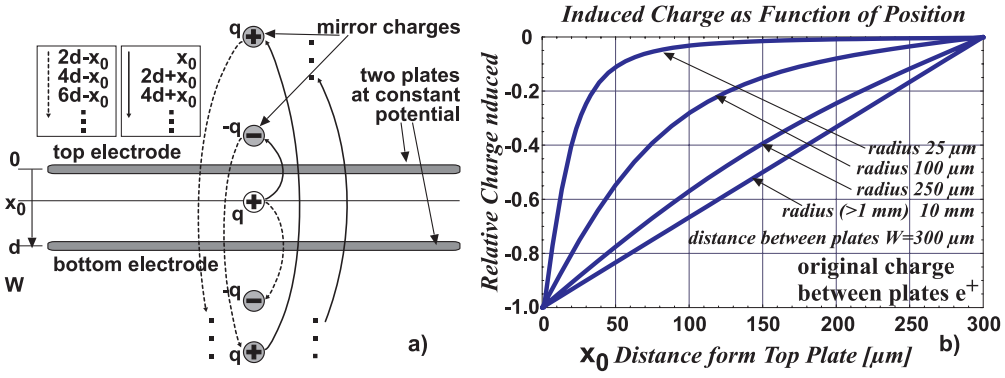

Figure 3-2: (a) Calculation of the induced charge in a plate using image charge method for a single fixed positive charge between two conductive plates, (b) Induced charge on the top plate as a function of the position of the single charge between the plates for different radii of the plate.

The similar analysis can be done to derive the charge induced on the bottom plate. Some example results obtained from a numerical summation from equation (3-14) are shown in Figure 3-2b. The plot shows the induced charge on one plate as a function of the distance x_0 of the original charge carrier from this plate. A typical distance d=300 µm between the plates was fixed for the numerical calculation. The curves in Figure 3-2b are plotted for different radii rad, over which the charge is collected. For the case, when the size of collecting electrode is significantly larger than the distance between plates, the induced charge on the

top and on the bottom plates satisfies with a good approximation the linear relations given by equation (3-15). The induced charges on both plates sum to the magnitude of charge between the plates, thus the charge is conserved

$$q_{ind}^{top,two} = q\left(\frac{x-d}{d}\right) \quad \text{and} \quad q_{ind}^{bot,two} = -q\frac{x}{d} \quad \text{with} \quad q_{ind}^{top,two} + q_{ind}^{bot,two} = -q\,. \tag{3-15}$$

Considering a hole and an electron created at the position x_0, and moving towards the top and bottom electrode, respectively, the carrier position as a function of time is calculated for the fully depleted detector from equation (3-9), obtaining

$$x(t) = \frac{d}{E_0'}\left(E_0' + E_1' - \left(E_0' + E_1' - E_0'\frac{x_0}{d}\right)e^{(+/-)\frac{\mu_{p,n}E_0}{d}t}\right) \quad (+)\text{holes} \quad (-)\text{electrons}\,. \tag{3-16}$$

Thus the charge induced on the top electrode due to moving single charge carriers are given for holes and electrons, respectively:

$$q_{ind,hol}^{top}(t) = \frac{q}{E_0'}\left(E_1' - \left(E_0' + E_1' - E_0'\frac{x_0}{d}\right)e^{\frac{\mu_p E_0}{d}t}\right) \quad \text{for holes} \quad 0 \le t \le \tau_{coll,p}\,, \tag{3-17}$$

$$q_{ind,ele}^{top}(t) = -\frac{q}{E_0'}\left(E_1' - \left(E_0' + E_1' - E_0'\frac{x_0}{d}\right)e^{-\frac{\mu_n E_0}{d}t}\right) \quad \text{for electrons} \quad 0 \le t \le \tau_{coll,n}\,. \tag{3-18}$$

The total charge is the convolution of the charges by all generated charges inside the detector, which is calculated by

$$q_{ind,total}^{top}(t) = \frac{q}{E_0'}\int_0^d Q(x_0')\begin{pmatrix}\left(E_0' + E_1' - E_0'\frac{x_0'}{W}\right)e^{-\frac{\mu_n E_0}{d}t} - \\ -\left(E_0' + E_1' - E_0'\frac{x_0'}{W}\right)e^{\frac{\mu_p E_0}{d}t}\end{pmatrix}dx_0' \quad \begin{matrix}0 \le t \le \tau_{coll,n} \\ 0 \le t \le \tau_{coll,p}\end{matrix}\,, \tag{3-19}$$

where $Q(x)$ is the distribution of the generated charge along the detector depth. The current through the electrode is calculated by differentiating the total charge and the observable signal is obtained by the response of the amplifying chain $V(t)$:

$$i_{ind,total}^{top}(t) = \frac{dq_{ind,total}^{top}}{dt} \quad \text{and} \quad V(t) = h_{amp}(t) * i_{ind,total}^{top}(t)\,, \tag{3-20}$$

where $h_{amp}(t)$ is the pulse response of an amplifier. Since electrons and holes move in opposite directions, they induce current of the same sign at a given electrode, despite of their opposite charges.

The image charge method is useful to solve charge collection in architectures with plane electrodes. In the general case of an arbitrary configuration of any number of charge collecting electrodes, the induced charge is determined applying Ramo theorem [41]. The example of application of this rule to a microstrip detector, described in Chapter 3.3.1, is shown in Figure 3-3. The electric field inside the detector is a superposition of field contributions due to each electrode. The electric field inside a detector is almost uniform, except in the immediate vicinity of the strips where electric lines bend to the electrodes. The electric fields determine the charge trajectory and velocity. The charge induced on collecting electrodes is calculated from the weighting potential, which is determined for each electrode for which signal is to resolve. The signal-weighting field depends only on geometry and determines how charge motion couples to a specific electrode. It is determined by applying unit potential to the signal i.e. measurement electrode and 0 to all others. Generally, the signal weighting potential is different than the electric field distribution, only in two-electrode configurations the electric field and the weighting field have the same form. An example of the signal weighting potential distribution is shown in Figure 3-3b for a single electrode of the microstrip detector.

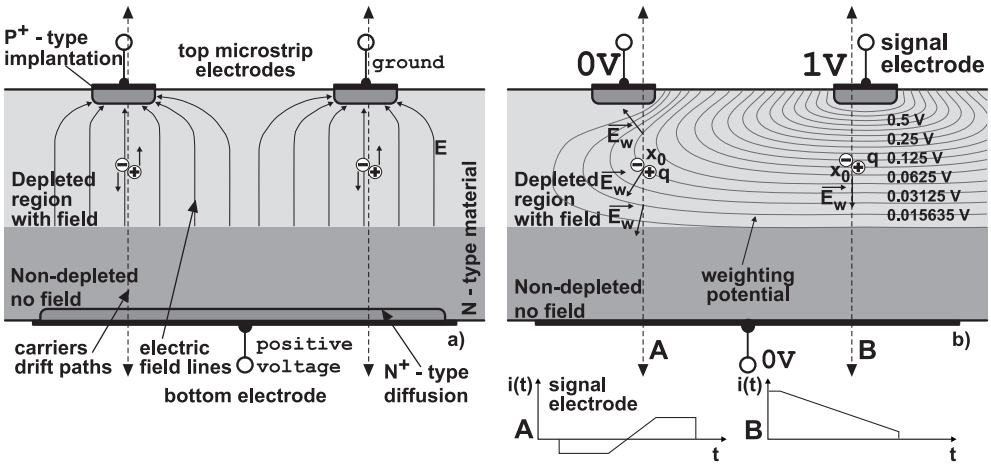

Figure 3-3: (a) Electric field in a segmented detector as a superposition of fields due to each electrode, (b) example of weighting field in a segmented detector.

The Ramo theorem states that the amount of induced charge q_{ind} is given by the product of the charge placed in a given point between electrodes and the signal weighting potential at this point. For a charge q moving along any path from the position 1 to the position 2, the

net induced charge on the electrode k is

$$\Delta q_{ind}^{top} = q\left(\Phi_k(1) - \Phi_k(2)\right), \tag{3-21}$$

where $\Phi_k(x)$ is a signal weighting potential determined for the electrode k at the position x in space. The instantaneous current through the electrode k can be expressed in terms of a weighting field determined for this electrode

$$i_k(t) = -q\vec{v}\left(\vec{r}\right)\frac{d\Phi_k}{d\vec{r}} = -q\vec{v}\left(\vec{r}\right)\overrightarrow{E_k}, \tag{3-22}$$

where $\vec{v}$ is the velocity of motion of the generated charge carrier and $\vec{r}$ is the position in space. The net effect, of both positive and negative charge carriers motion, is a negative current at the positive i.e. top electrode and a positive current at the negative electrode, due to both. In general, if moving charge does not terminate on the signal electrode, the signal current is induced on other electrodes but the current changes sign and integrates to zero, as it is shown in Figure 3-3b. The current cancellation on non-collecting electrodes relies on the motion of both electrons and holes. Usually, the signal weighting potential is strongly peaked near the signal electrode, thus most of the charge is induced when the moving charge gets near or terminates on the signal electrode.

In the case of a partially depleted detector the depletion zones due to each charge collecting diodes can be very shallow and separated on the same substrate. Hence, electric fields as a result of each electrode are also separated, and the non-depleted part can be considered as a constant potential volume. The charges originating in this part may diffuse until they reach the region with electric field of one of the collecting electrodes. In this case the signal weighting potential and the electric field are the same. Thus, the signal is only induced on the electrode on which the charge terminates.

3.2.3 Basic Considerations of Noise in Integrated Circuits

The figure of merit in detector systems is the SNR. The resolution is dependent on detector geometry and its material properties and improves with higher SNR [42]. Physical processes leading to charge generation limit the magnitude of signal. Thus, careful optimisation of noise performance of the system is required to provide satisfactory SNR. There are many sources that can cause noise in integrated circuits and the detector, such as power supply fluctuation, electro-magnetic interference, substrate coupling etc. Often these

external interferences can be reduced to acceptable levels, either by proper circuit design practice, or by carefully applying shielding and grounding techniques. There are, however, intrinsic noise sources in integrated circuits that are hard to suppress. Generally, two mechanisms contribute to the total noise of integrated circuits. The first effect of carrier velocity fluctuations is observed as thermal noise of the device. The second process is due to fluctuations in the number of charge carriers and leads to shot noise and excess noise, with latter referenced as flicker or $1/f$ noise. Considering N carriers of charge moving with a velocity v through a sample of length l yields the induced current I at the ends of the sample, which fluctuations $\overline{dI^2}$ are expressed by two noise components according to:

$$I = \frac{N\,q\,v}{l} \quad \text{and} \quad \overline{dI^2} = \left(\frac{Nq}{l}\right)^2 \overline{dv^2} + \left(\frac{qv}{l}\right)^2 \overline{dN^2}\,. \tag{3-23}$$

Two terms, describing current fluctuations in equation (3-23), are added in quadrature, since they are statistically uncorrelated.

Thermal noise and shot noise are both white noise sources with constant power per unit bandwidth, which is expressed by

$$\frac{dV_{noise}^2}{df} = v_n^2 = \text{constant} \quad \text{or} \quad \frac{dI_{noise}^2}{df} = i_n^2 = \text{constant}\,, \tag{3-24}$$

whereas, the spectral density of excess noise depends on the frequency according to

$$\frac{dV_{noise}^2}{df} = v_n^2 \propto \frac{1}{f^{\alpha}} \quad \text{or} \quad \frac{dI_{noise}^2}{df} = i_n^2 \propto \frac{1}{f^{\alpha}}\,, \tag{3-25}$$

where f is the frequency and the parameter α is typically between 0.5 and 2. The total noise in the system depends on the bandwidth of the whole signal chain. The total noise power at the output of a voltage amplifier characterised by the frequency dependent gain $H_{amp}(f)$ is calculated integrating over the noise power by

$$v_{on}^2 = \int_0^{\infty} v_n^2(f)\,H_{amp}(f)\,df\,. \tag{3-26}$$

The most common example of noise due to velocity fluctuations is the thermal noise of any resistive region e.g. polysilicon resistors, a MOS transistor channel in strong inversion etc. It has zero mean, and is represented either as a voltage source in series or as a current source in parallel with a resistor. Its spectral noise densities are calculated by

$$\frac{dV_{noise}^2}{df} = v_{n,th}^2 = 4\,k\,T\,R \quad \text{and} \quad \frac{dI_{noise}^2}{df} = i_{n,th}^2 = \frac{4\,k\,T}{R}, \tag{3-27}$$

respectively, where k is Boltzmann constant and R is resistance.

The noise due to fluctuations in the number of charge carriers is the shot noise. It occurs whenever charge carriers are injected into a sample volume independently of one another. An example is the current flow in a semiconductor diode or a bipolar transistor, where charge carriers are injected from one region to another passing through a potential barrier. It has zero mean, and is often represented by a current source in parallel with the DC current of the noisy element. Its spectral noise current density is given in this case by

$$i_n^2 = 2\,q\,I, \tag{3-28}$$

where I is the continuous current conveyed by a diode.

Flicker noise is caused by traps due to crystal defects and contaminants in electronic devices. Charge carrier number fluctuations are caused by these traps randomly capturing and releasing carriers. Flicker noise is associated with continuous currents flowing through resistive regions and through potential barriers. Flicker noise is characterised by a zero mean and a power spectral density proportional to the current flowing through an electronic device.

3.2.4 Noise in Active Devices: Diodes and MOS Transistors

The dominant sources of noise in a diode are shot noise and $1/f$ noise due to the bias current. Diodes used as active detector elements are operated under reverse bias and the noise results from some dark currents conveyed through the device. Under the detector exposure to the source of light or other type of ionising radiation, additional noise contributions of the current i_{ph} of generated charge carriers have to be additionally taken into account. The two noise current sources of the shot noise and the $1/f$ noise are statistically independent and are expressed correspondingly by

$$i_{shot}^2(f) = 2\,q\left(i_{ph} + i_{dc}\right) \quad \text{and} \quad i_{1/f}^2(f) = a\frac{i_{dc}^c}{f}, \tag{3-29}$$

where the exponent c is $0.5 \le c \le 2$, and a is a constant that depends on the physical characteristics of the diode and i_{dc} is the constant bias current of the diode. Shot noise is caused by the electrons that randomly cross the depletion region. On the other hand, flicker

noise is caused by fluctuations in the surface recombination velocity and by fluctuations in bulk carrier mobility. The flicker noise is proportional to the density of surface states. In the reverse biased diodes, only dark currents generate this noise. The total current, including both, the dark current and the current induced by radiation, generates the shot noise.

The noise mode of a MOS transistor is more complicated, since it depends on the operation condition of this device. For a MOS transistor biased at strong inversion, the transistor channel is resistive, thus the dominant source of noise is thermal noise. In the weak inversion region, the dominant source of noise becomes shot noise. In addition to the thermal or shot noise, a MOS transistor also suffers from flicker noise, which results mainly from the traps in the gate oxide. Noise in a MOS transistor is modelled by two statistically independent current sources for the thermal or shot noise and for the flicker noise, which are connected in parallel with the drain current i_{ds}. Usually, the saturation and the linear region of a MOS transistor operation are considered separately.

The thermal or shot noise source is modelled as a white noise with zero mean and power spectral density given by

$$i^2_{d,th,sat}(f) = 4\,k\,T\,n\,\gamma\,g_m\,, \tag{3-30}$$

$$i^2_{d,th,lin}(f) = 4\,k\,T\,g_{ds,lin}\,, \tag{3-31}$$

for the saturation and the linear operation region, respectively. Consecutively, the flicker noise source has zero mean and a power spectral density given by

$$i^2_{d,1/f,sat}(f) = \frac{K_F\,g_m^2}{C_{ox}\,W\,L}\,\frac{1}{f}\,, \tag{3-32}$$

$$i^2_{d,1/f,lin}(f) = \mu^2_{n,p}\,\frac{K_F\,W}{L^3}\,V^2_{DS}\,\frac{1}{f}\,, \tag{3-33}$$

where, the first and the second formula represent a MOS transistor in the saturation and linear region, respectively. In formulas (3-30) - (3-33), g_m, $g_{ds,lin}$ are the small signal transistor channel transconductance and conductance parameters, respectively, n is a parameter combining small-signal gate and bulk transconductances, which is proportional to the inverse of the sub-threshold slope $\mathbf{log}(I_{DS})$ versus the voltage V_{GS}, γ is a complex function of the basic transistor parameters and bias conditions, K_F is a flicker noise coefficient. Under the ideal conditions, γ changes its value from $1/2$ to $2/3$ passing from weak to strong inversion.

For the real device, the use of the parameter γ allows to include some excess noise, which is mainly due to gate and bulk spread resistances. This effect is taken into account by including into γ a scaling factor Γ, varying γ from $1/2\Gamma$ to $2/3\Gamma$ from weak to strong inversion [43] using the following formula

$$\gamma = \left(\frac{1}{2} + \frac{1}{6} \frac{u}{f^2(u)} \right) \Gamma , \tag{3-34}$$

where $f(u)$ is given by

$$f(u) = \frac{1}{2}\left(\sqrt{1+4u} + 1 \right) \quad \text{with} \quad u = \frac{I_{DS}}{\left(\frac{W}{L} \right) \mu_{n,p} C_{ox} \left(2 n V_T^2 \right)}, \tag{3-35}$$

where W and L are the effective channel width and length, respectively, $\mu_{n,p}$ is the mobility of electrons and holes in the channel for an NMOS and PMOS device, and C_{ox} is the gate oxide capacitance per unit area. The parameter u is an indication of the degree of inversion of the channel. The transconductance g_m in strong inversion and weak inversion, respectively, can be further expressed as a function of the bias voltages

$$\begin{aligned} g_{m,strong} &= \left. \frac{\partial I_{DS}}{\partial V_{GS}} \right|_{\substack{V_{DS}=V_{DS,0} \\ V_{GS}=V_{GS,0}}} = \\ &= \mu_{n,p} C_{ox} \frac{W}{L} \left(V_{GS,0} - V_T \right) \left(1 + \lambda V_{DS,0} \right) = \sqrt{\mu_{n,p} C_{ox} \frac{W}{L} I_{DS} \Big|_{\substack{V_{DS}=V_{DS,0} \\ V_{GS}=V_{GS,0}}}} \end{aligned} , \tag{3-36}$$

$$g_{m,weak} = \left. \frac{\partial I_{DS}}{\partial V_{GS}} \right|_{\substack{V_{DS}=V_{DS,0} \\ V_{GS}=V_{GS,0}}} = \frac{q I_{DS}}{n k T} , \tag{3-37}$$

where, V_{DS} is the drain source voltage, V_{GS} is the gate source voltage; V_T is the transistor threshold voltage and λ is the channel length modulation coefficient. Similarly, the conductance $g_{ds,lin}$ is given by

$$g_{ds,lin} = \left. \frac{\partial I_{DS}}{\partial V_{DS}} \right|_{\substack{V_{DS}=V_{DS,0} \\ V_{GS}=V_{GS,0}}} = \mu_{n,p} C_{ox} \frac{W}{L} \left(V_{GS,0} - V_T \right) , \tag{3-38}$$

The drain current in weak inversion is an exponential function of the bias voltages and is given by

$$I_{DS} = \frac{W}{L} I_{DO} e^{\frac{qV_G}{nkT}} \left(e^{-\frac{qV_S}{kT}} - e^{-\frac{qV_D}{kT}} \right), \tag{3-39}$$

where I_{DO} is a constant that depends on the transistor threshold voltage and V_G, V_S, V_D is potentials of the gate, source and drain terminal with respect to the bulk, respectively. The transition point, where equation (3-38) is valid occurs at

$$I_{DS} \le \frac{n-1}{e^2} \frac{W}{L} \mu_{n,p} C_{ox} \left(\frac{kT}{q} \right)^2, \tag{3-40}$$

when $V_{DS} > 3kT/q$.

The design of integrated circuits demands a careful noise optimisation to provide satisfactory SNR. The noise performance is of paramount importance for the design of low-noise front-end parts of read-out circuits. Modern deep sub-micrometer processes, stepping into the common use in designs of front-end circuits, need special attention of designers. Noise coefficients like K_F or Γ are used in standard noise analyses as constants characterising given fabrication process. Effectively, they depend on the work regime of the MOS transistor, i.e. if it is weak, moderate or strong inversion, as well as on the device dimensions, especially on the gate length. Some departures from standard, time-honoured models used in noise circuit analyses and SPICE simulations were observed in detailed noise measurements done for a 0.25 μm process [44]. Some new effects found in measurements can be included in the noise analysis using still standard formulas, but usually constant noise parameters should be adjusted as a function of the channel inversion strength and transistor dimensions. According to measurements, the Γ factor in weak and moderate inversion for NMOS transistors is close to the ideal value of one for all the gate lengths, but the K_F parameter increases steeply for gates shorter than 0.6 μm, reaching a 3.5 times higher value for the shortest gates achievable in a given process comparing to long transistors. For long gate transistors, changing operation region to strong inversion results in three times higher Γ factor. The Γ factor becomes still worse for short gate devices operated in strong inversion under high bias current conditions. Moreover, some additional increase of the K_F parameter is observed in strong inversion, but in contrast to the weak inversion operation, in this case longer gate transistors are more concerned. The effect of noise dependence on operation region and dimensions of MOS devices has to be taken into account for noise-optimised

designs of read-out circuits. In the case of Monolithic Active Pixels Sensors described in Chapter 3.3.5, the noise coefficient scaling translates to trade off between the charge-to-voltage conversion gain and dimensions of the input MOS transistor.

3.3 Different Types of Semiconductor Position Sensitive Detectors

3.3.1 Microstrip Detectors

Microstrip detectors [45, 46] are made of a large number of identical detector structures in a plane. They are manufactured in a form of a splitted up into many strips metal electrode placed on a common support in order to obtain a device with high resolution in one dimension. Each detector element consists of reverse biased strip-shaped p-n diode, in which the electric field separates the electrons from the holes. The charge carriers are guided to the strips on which the signal can be probed. Usually, the strips are formed by highly doped p-type implants, while the thick active volume of the detector is a high resistivity n-type region. Microstrip detectors were proposed in early 80's, and since that time they are used as position sensitive devices in most particle physics experiments requiring high precision tracking. They provide one-dimensional information about the particle track location*. Figure 3-4 shows a partial view of the DELPHI experiment vertex detector with cylindrical layout of microstrip detectors, along with precursory pixel detectors installed at the end-caps.

Microstrip detectors are usually segmented in 10 μm to 50 μm wide strips, which are several centimetres long. Due to large capacitance per strip, which is typically about 1 pF/cm, they require low-noise read-out circuitry. Various read-out schemes have been successfully applied. The read-out chips can be bonded on one side or on both sides of a detector. Every strip can be connected to its read-out channel or intermediate strips can be left floating being only capacitively coupled to the neighbouring strips. Depending on particular requirements of an experiment, information on the signal magnitude provided by the read-out electronics either can be sufficient represented in a binary way with fired up channels whose signal crosses a threshold or is proportional to the signal height in a pure analogue way or uses several quantization levels of analogue-to-digital conversion.

* The actual track location is obtained after applying one of many existing track determination algorithm consisting for example in calculation of the centre of gravity of the charge collected on the adjacent strips.

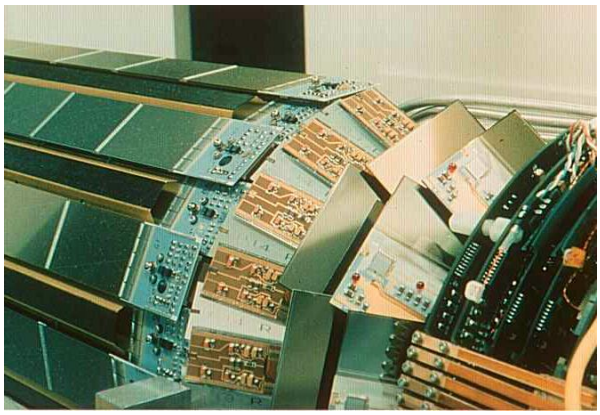

Figure 3-4: Partial view of the vertex detector (from DELPHI collaboration).

The read-out electronics can either be AC or DC coupled* to the detector, the latter requires the front-end electronics capable to compensate the leakage current of the detector. Depending on the actual detector geometry, which consists mostly in a combination of the read-out and strip pitches, and an algorithm used for processing signals from the detector, the spatial resolution of a single plane detector can be as good as a few micrometers in one dimension. Combining several layers of microstrip detectors can provide tracking systems characterised by a spatial resolution as good as 1 μm [47]. A schematic view of a single-sided, AC-coupled strip detector with interleaved strips is shown in Figure 3-5. The adjacent strips are capacitively coupled by inter-strip capacitances C_{ip}.

A solution, allowing to achieve two co-ordinate position information, can rely on two microstrip detectors mounted back to back with strips on both detectors rotated against each other. Another approach consists on implanting n-doped strips onto the backside of a detector. In this case, n-type strips must be rotated by some angle with respect to the topside p-type strips. The n-type strips form ohmic contacts to the active volume. Thus, they have to be separated by p-type channel stoppers. A schematic view of a double-sided microstrip detector is shown in Figure 3-6. In either case when microstrip detectors are used, only single tracks are unambiguously reconstructed.

* AC coupling of a detector to a readout electronics is realised through capacitances between P^+ or N^+ strips and metal lines integrated directly on a detector. The strips are usually biased through high resistance polysilicon resistances, using punch-through effect or a FOXFET (Field Oxide Field Effect Transistor) element. The strips in the case of DC-coupled detectors are biased directly through the associated channels of the read-out electronics.

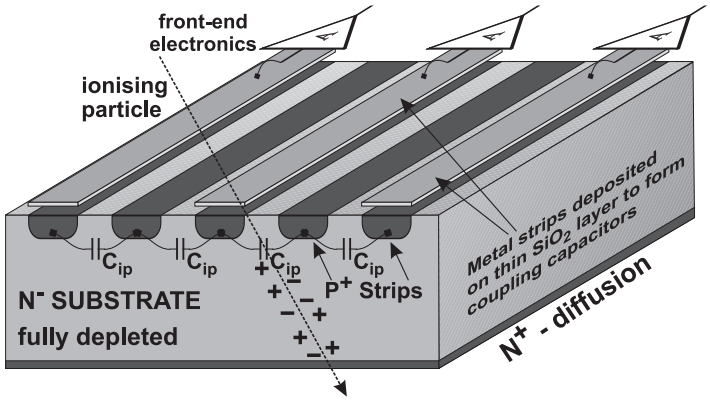

Figure 3-5: Schematic view of a single-sided, AC-coupled strip detector with interleaved strips.

In the case of n tracks there are n! possible combinations of the hits in the individual planes, what introduces important ambiguities. However, combining several of these double microstrip planes with an iterative track finding algorithms, the ambiguities can partially or fully be resolved and the tracks reconstructed. The advantage of using double-sided detectors against the combination of two planes of single sided detectors is a significant reduction of material the particle has to traverse, in which it can suffer from multiple Coulomb scattering.

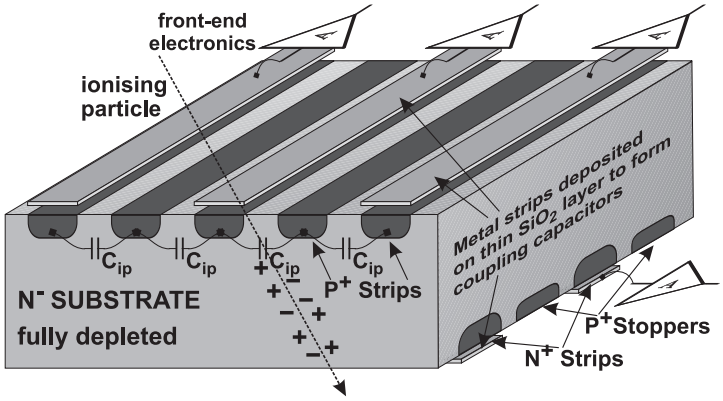

Figure 3-6: Schematic view of a double-sided, AC-coupled strip detector with interleaved strips.

3.3.2 Drift Detectors

The principle underlying the drift detector is a drift channel created by a special biasing scheme of implants on both sides of the detector [48]. A schematic view, without an external

biasing schemes used for forming the potential gradient, is shown in Figure 3-7. The carriers of one type, which are usually electrons due to their higher mobility, first drift towards the middle of the structure and afterwards towards the collection electrodes, which can be segmented in a form of n^+-type pads. The holes are collected by one of a biasing p^+-type strip. The electrons induce a charge on the collecting pads. However, the weighting fields of the charge collecting electrodes is significant only in their very close vicinity, due to the shielding effect of the bias electrodes. Thus the signal is sensed only when the electrons are close to the n^+ electrodes. The silicon drift detector provides unambiguous two-dimensional track information. The first dimension is measured through the time between the incidence of the particle, determined by another detector, and the arrival of the electrons at the collection electrode. The second co-ordinate is given by the distribution of charge between the different pad electrodes. Drift Detectors require careful temperature control because of the strong dependence of the drift velocity on temperature: $v_{drift} \propto T^{-2.4}$. The spatial resolution obtainable with drift detectors is of the order of a few micrometers, which is comparable to that of microstrip detectors. This kind of device is best suited for experiments with very high particle multiplicities, however it deals only with low event rates.

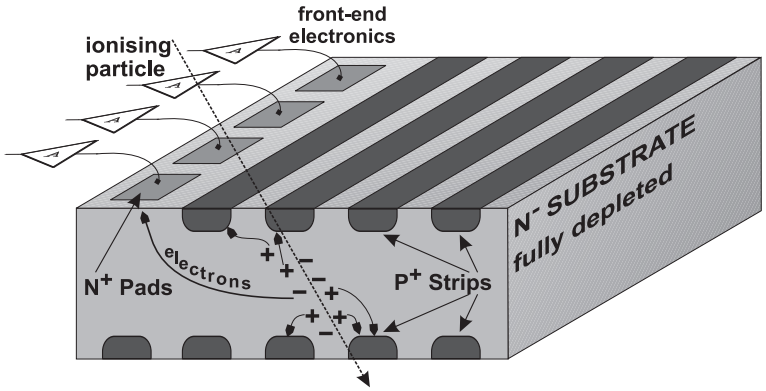

Figure 3-7: Schematic view of a drift detector.

3.3.3 Classical Pixel Detectors

3.3.3.1 Pad Detectors

Pad detectors are arrays of independent, p-n diodes (pads) implemented adjacently on one common substrate. In early days, arrays of separate discrete silicon diodes connected to

individual read-out channels were proposed for tracking. Each detection element was typically several mm^2 in size and was connected to its individual signal-processing channel via metal routing lines on top of the detector. The connection pads, to which the read-out electronics was attached, were usually placed at each side of a detector. The schematic view of a pad detector is shown in Figure 3-8. These days, pad detectors are used in Hybrid Photon Detectors (HPD) [49]. The accelerated electrons emitted from a photo-cathode impinge on the back surface of the silicon pad detector in order to minimise their energy loss in the aluminium contacts. The pad detectors for this application are fabricated in the form of a 300 μm thick round silicon disk of about 5 cm active diameter and comprise 2048 pads of 980 × 980 μm size.

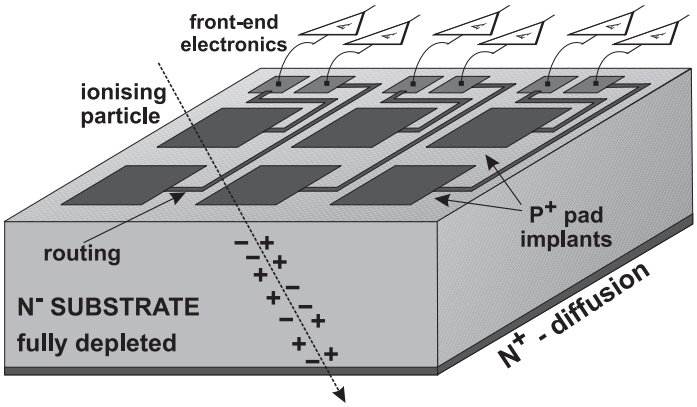

Figure 3-8: Schematic view of a pad detector.

3.3.3.2 Hybrid Pixel Detectors and Pixel Front-End Electronics

Hybrid Pixels Detectors use high resistivity substrate like microstrip detectors. The possible size of a pixel is determined by the size of the readout chip. Hybrid Pixel Detectors were used for the first time in the WA97 and NA50 heavy-ion experiments at CERN. Their intensive growth was initiated and is driven by the development for the LHC detectors, where very fast and radiation hardened devices are required [50, 51]. Some requirements and specification for past and future High Energy Physics experiments are shown in Table 3-6.

The detector part consists essentially of a microstrip detector structure, each strip being subdivided into some number of short pieces, which constitute the pixels. The sensor array and the matching read-out chip are processed independently and are connected together only in the final step. In this way the material and processes can be individually optimised for the

actual purpose i.e. detector and electronics.

Table 3-6: Requirements and specification for the Hybrid Pixel Detectors in some High Energy Physics experiments.

Experiment	Surface area [m^2]	Number of channels	Pixel size [μm^2]	Spatial resolution ($r\phi$) [μm]	Occupancy at nom. luminosity [#hit/BX]	Maximum neutron fluence [cm^{-2}/10yrs]	Maximum ionising dose [Mrad/10yrs]
DELPHI*	0.15	1.2×10^6	330×330	80÷100	-	-	>0.01
ATLAS†	2.29	140×10^6	50×400	~12	10^{-4} /pixel	10^{15}	20
CMS‡	1.18	80×10^6	150×150	<15	3.3×10^{-4}	10^{14}	35
ALICE§	0.23	14.4×10^6	50×425	~12	10^{-2}	10^{12}	0.12

This approach makes it possible to achieve fast enough readout and radiation hardness compatible with the LHC environment. The detector substrate is high resistivity silicon, although other materials than silicon, e.g. diamond, are also considered. The readout electronics is built in an industrial CMOS foundry and it can be similar in architecture to the classical front-end topology for microstrip detectors. The connection of the detector and the read-out electronics is customarily done by means of the flip-chip bonding technique, where small balls of solder, indium or gold establish the electrical and mechanical connection between each detection element and its read-out circuit.

Hybrid detectors have the disadvantage of high complexity of millions of interconnections and they introduce extra material in the active area. Moreover, Hybrid Pixels Detectors are characterised by the relatively high power dissipation reaching a few hundred mW/cm^2 and relatively large size of a single cell needed to integrate required complex functionality of the readout circuitry.

The new ideas for capacitively coupled Hybrid Pixel Detectors inheriting from microstrip detectors with interleaved strips were recently proposed [52]. This solution, based on the microstrip detectors with capacitive charge division, allows to improve the spatial resolution leaving enough space for each channel to integrate the read-out electronics. In the construction of this new detector, the read-out pitch, fitting area needed for read-out

* DELPHI stands for DEtector for Lepton, Photon and Hadron Identification.

† ATLAS stands for A Toroidal LHC Apparatus.

‡ CMS stands for Compact Muon Solenoid.

§ ALICE stands for A Large Ion Collider Experiment.

electronics, was proposed to be n (n=2, 3, 4) times larger than the physical pitch of pixel diodes. A schematic cross sectional view of a hybrid pixel detector with interleaved, capacitively coupled pixels for n=3 is shown in Figure 3-9.

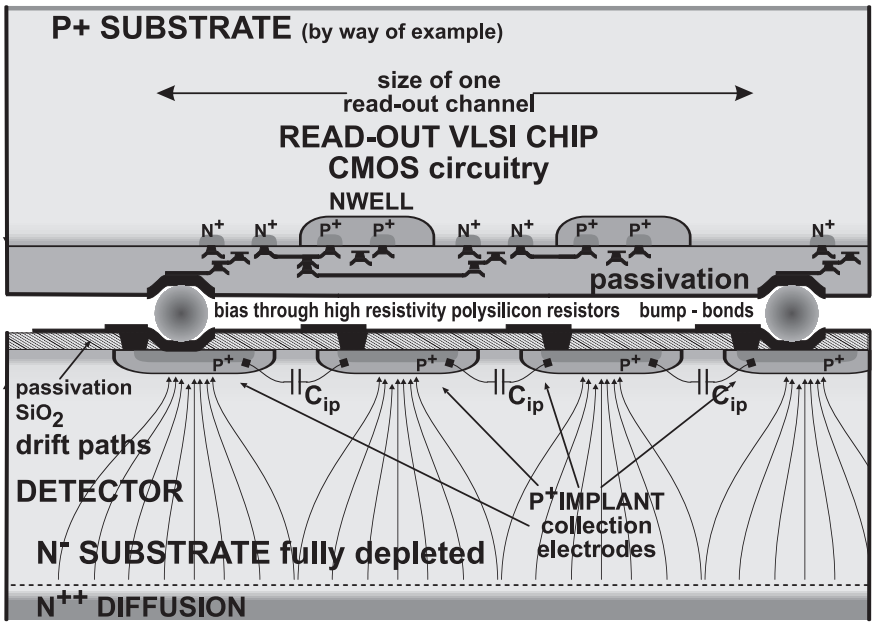

Figure 3-9: Cross sectional view of a hybrid pixel detector with interleaved pixels showing the detector chip (bottom) bump bonded to a readout VLSI chip (top).

In such a configuration, the charge carriers created underneath an interleaved pixel induce a signal on the output nodes, capacitively coupled to the interleaved pixel. The ratio between the inter-pixel capacitance C_{ip} an the pixel capacitance to the back-plane plays a crucial role in the detector design, as it defines the signal amplitude reduction at the output node and therefore the maximum sustainable number of interleaved pixels. Results obtained, with a detector featuring a 200 μm readout pitch and the division coefficient n=4, with an infra-red beam light source [53] show an average spatial resolution of about 6.4 μm achieved by applying the position reconstruction algorithm which takes into account charge sharing mechanism. The η distribution function, defined as the pulse height on the reference pixel normalised to the cluster pulse height, shows that achieving spatial resolution demanded by Future Linear Colliders will require a pixel pitch of about 25 μm for n=4. From many reasons, e.g. care for proper biasing schema and significantly shrunk space for readout electronics; this is quite far from a simple scaling of structures with current, looser layout.

Extensive studies are required in order to fully profit from advantages of Hybrid Pixel Detectors in applications demanding very precise tracking capabilities.

The architecture of the very elementary pixel cell read-out electronics is shown in Figure 3-10 [54]. This structure aims to detecting the presence of signals stamped as hits, when the charge exceeds a preset threshold. The pixel detector is represented as an array of p-n diodes realised on an n-type substrate. The signal generated by the detector is fed into a charge sensitive preamplifier and then to the pulse shaping amplifier, a shaper. Usually pixel detectors are DC coupled with the read-out electronics, which has to be able to compensate leakage current of the detecting diode. The preamplifier integrates the charge Q generated in the detector onto a small feedback capacitance C_f giving rise to a voltage step with amplitude Q/C_f at the output. The output amplitude is essentially insensitive to the actual capacitance value at the input of the preamplifier, although this capacitance determines the noise performance of the preamplifier. The preamplifier and the shaper form the linear section of the read-out circuitry. The shaper is followed by a pulse-processing unit, which can be either a simple discriminator for binary event detection built with a comparator or a sample and hold circuit to store analogue pulse information. The comparator transition is stored in a local flip-flop or latch type memory or in a shift register to wait for the trigger arrival. The charge-sensitive preamplifier is usually constructed around a single inverting stage, whose transfer function can be represented as g_{mMin}/sC_0, where g_{mMin} is the transconductance of the input device and C_0 the internal capacitance accounting for the limitation of the gain-bandwidth product. The capacitance C_d represents the total capacitance of the pixel, and C_i is the input capacitance of the preamplifier. The current fed from the detector to the preamplifier can be divided into two sources: the current $i(t)$ due to a signal induced on the pixel, and the constant leakage current I_{leak}. The shot noise associated to the detector leakage current and the current output noise of the leakage current compensation circuit are two sources of parallel noise in the system. The noise of the preamplifier is represented by the voltage input-referred noise source v_i^2 and is a serial noise source.

One of the crucial aspects in the cell design is the leakage current compensation, which may require a dedicated low frequency feedback loop, similar to that used for DC-coupled microstrip detectors [55, 56] and placed in parallel to the loop for dynamic charge reset. A

second critical aspect is a pixel-to-pixel dispersion in the comparator threshold levels. This is problem usually solved by adding local trimming capability of threshold levels.

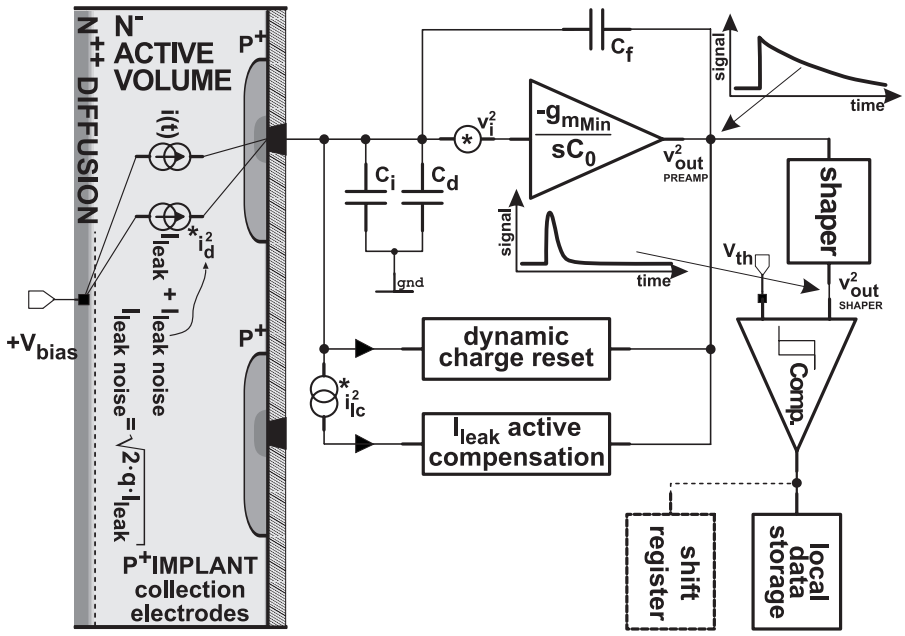

Figure 3-10: Elementary pixel cell in hybrid approach for pixel detector.

CMOS technologies are usually chosen due to their high integration density, low power consumption and the possibility of combining the analogue and digital circuits on the same chip at the advantageous cost. Using modern sub-micrometer processes it is possible to integrate complex and fast circuitry in small areas close to the detector. Usually the area occupied by readout electronics determines the minimum size of the single pixel. But, in the case of Hybrid Pixel Detectors, each elementary cell can be considered as an independent and fully functional detecting element, resulting in fully parallel handling of signals from each implemented adjacently charge-collecting diode. Such a mode of signal processing allows fast operation of the detector, and the implementation of an efficient data sparsification prompts easy solutions for the operation of the vertex detector which makes use of the trigger signal delivered after preliminary processing of a particular event and the decision on its usefulness for physics. The data sparsification results in a significant reduction of the data transferred to the data acquisition system for recording for further analysis.

Another important aspect of the detector design is the noise. The target noise performances must be guaranteed under the constraints of low power dissipation and be

retained upon the absorption of the total radiation dose expected during the lifetime in a physics experiment. The noise of a detection system is usually expressed as the total equivalent noise charge (ENC)*. This unit allows easy comparison with the generated signals expressed in a number of charge carriers induced on readout electrodes. To achieve small value of ENC, under constraints that apply to pixel front-end design, a large transconductance to the DC bias current and a high transition frequency at low currents are the essential requirements for the input device. In VLSI processes, these requirements are met either by a bipolar transistor of a small emitter periphery or by a short channel MOS transistor. The latter element is much more often used, which is mainly due to the wide availability and lower fabrication cost of CMOS processes. The detailed noise analysis performed for a classical configuration of the front-end circuitry for hybrid version of a pixel detector is presented in Appendix-A.

3.3.3.3 Charge Coupled Devices

The development of detectors exploiting Charge-Coupled Devices (CCDs) was driven by their use as photon detectors in the visible band. CCDs offering unambiguous two-dimensional spatial resolution were the first pixel detectors introduced in high energy physics applications at the CERN SPS in the NA32 fixed target experiment [57]. The spatial resolution of these first devices was about 5 μm and the achieved two-track resolution was in the order of 40 μm [58]. Then, CCDs were successfully used for the construction of the vertex detector for the Stanford Linear Accelerator Collider (SLAC) Large Detector (SLD) experiment [59, 60]. The single-track resolution of 4.6 μm was obtained. The slow repetition and low trigger rates of the SLC collider were setting up the ideal conditions for the use of CCDs. The CCDs at SLD consist of an array of $20 \times 20\ \mu m^2$ potential wells in which electrons released by the passage of a charged particle through the 25 μm depleted silicon are trapped. The potential of each well is controlled by a polysilicon gate and falls on a 2-μm deep buried channel, where the electrons are collected. The device is read out by sequentially changing the potential on three neighbouring gates in such a way that all charges are transferred in parallel from one row to the next, down the device. Charges in the last, bottom

* The equivalent noise charge, ENC, is defined as a ratio between the total r.m.s. value of noise at the output of the readout electronics and the signal amplitude due to a single electron.

row of the array are transferred into the adjacent linear register, from which they are shifted, one at a time, onto the output node to the charge sensitive amplifier realising charge-to-voltage conversion.

CCDs does not experience any dead time or any dead zone, and are continuously sensitive to the radiation, but require fairly long time for readout. The charge has to be serially shifted under one gate to the next across the rows and columns of pixels, and due to the large number of elements to go through, the readout time of the whole detector can reach hundred of milliseconds. This was not a problem for SLD, where the interaction rate is only about 1 Hz, but is a severe drawback of CCDs for new experiments at LHC or at Future Linear Colliders (e.g. TESLA). Another weak point of CCDs is their poor radiation hardness. They suffer from the post-irradiation diminution of a carrier lifetime and charge trapping occurring in numerous bulk transfers, which result in deterioration of the charge transfer efficiency. Consequently, only a fraction of the charge generated is available for the conversion to a voltage signal realised at the output node. It is worth highlighting that even very small charge transfer inefficiency can lead to the significant losses and smearing in the transferred charge. As an example, the efficiency of a single charge transfer in the order of 0.01% leads after 1000 transfers to 10% losses. This estimation takes into account charge spillage only in one direction and neglects transfers in the linear register occurring in a classical CCD.

In order to overcome problems of the limited read-out speed and to adapt the operation of the detector to deteriorated post-irradiation performance, a new generation of CCDs is under study. The research work includes a fast 50 MHz clocking, column parallel read-out and low temperature operation. A conceptual cross sectional view of a CCD detector featuring column parallel read-out capability in which bump pads are placed at the column ends to connect the device to the front-end chip, is shown in Figure 3-11. The readout chip receives the analogue signals from all columns in parallel as they are shifted out of the active area to buffer amplifiers. Furthermore, the new CCD detector will be less concerned by a multiple scattering effect deteriorating spatial resolution. It is proposed to have a form of less than 50 μm thick slabs of a varied size of 22×125 mm^2 and 13×100 mm^2 and containing 6.9×10^6 and 3.3×10^6 pixels, respectively. These detector planes are expected be used in construction of the TESLA vertex detector mounted as stretched, self-supporting elements

onto the ladder blocks [1, 61].

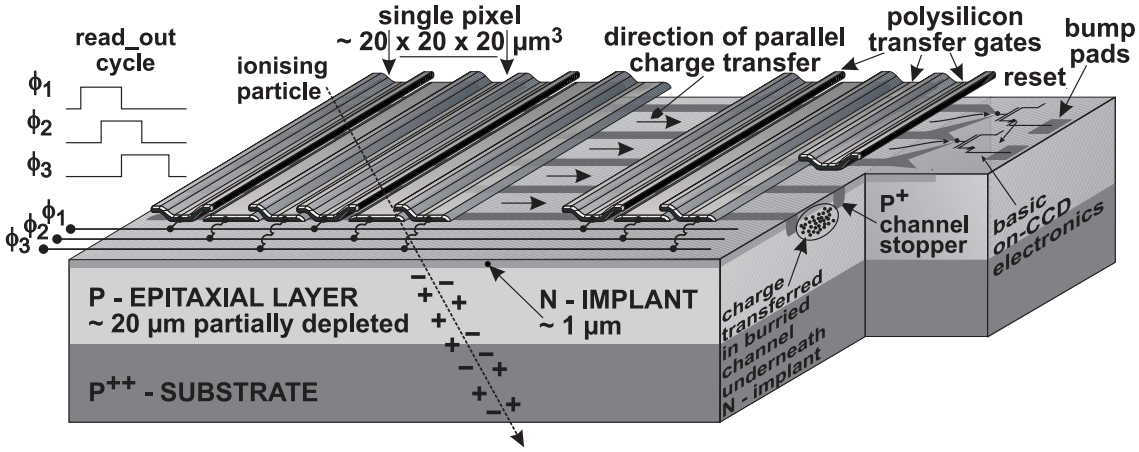

Figure 3-11: Cross sectional view of a column parallel CCD detector.

3.3.3.4 Monolithic Pixel Detectors

In a monolithic pixel detector, the signal processing circuits are placed in wells next to the charge collecting electrodes or are built into a thin silicon layer which is separated from the active detector volume by an insulating SiO_2 layer. The first and the second option are used in the case of a bulk semiconductor process and SOI (Silicon on Insulator) technology, respectively. Several groups have combined detector and its electronics onto the same substrate and used the high resistivity silicon as the fully depleted active volume of typically 300-µm thicknesses. The monolithic pixel detector design on a high resistivity substrate is complicated, since a dedicated, fabrication process must be used. In the bulk approach, the wells containing the read-out electronics shields the detection volume against the influence of the switching transistors and guide the charge carriers towards the collection electrodes. A fully functional monolithic pixel detector array of 10×30 pixels, measuring each $125 \times 34\ \mu m^2$ was produced using only PMOS electronics within the pixel and both types of complementary transistors at the periphery [62, 63, 64]. The device integrated a two-dimensional array of n-wells, containing the read-out circuitry in the high resisitivity p-type detector substrate. The wells were surrounded by collection diodes formed by highly doped p^+-type implants. A schematic view of this kind of detector is shown in Figure 3-12. The junction at the backside is common to all pixels and a double sided processing is required for the backside diffusion, which must not reach the edge of the detector to avoid shorts that can occur when dicing the wafer.

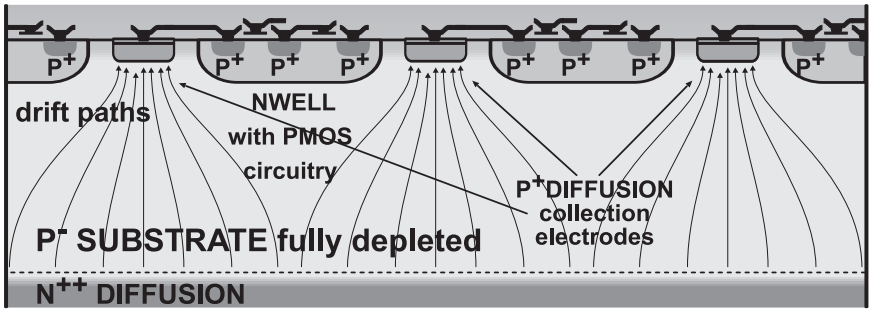

Figure 3-12: Cross sectional view of a monolithic pixel detector on a high resistivity substrate.

A schematic cross sectional view of a monolithic pixel detector realised in SOI technology is shown in Figure 3-13. The SOI option makes use of an isolating buried layer of oxide to separate the detection volume from the readout electronics.

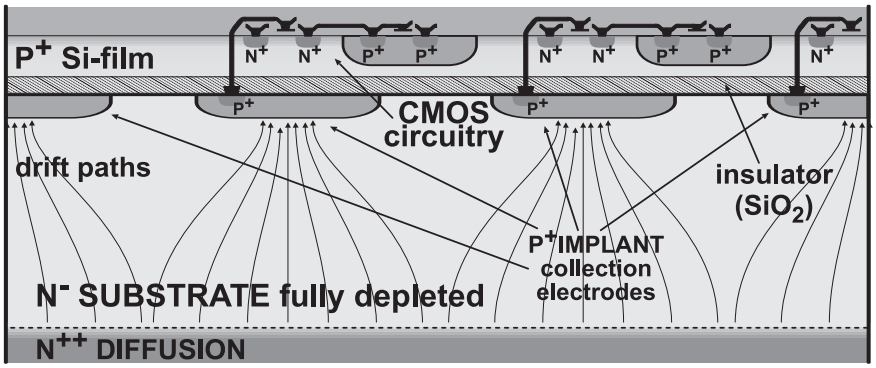

Figure 3-13: Cross sectional view of a monolithic pixel detector realised in SOI fabrication process.

SOI wafers for detectors were successfully fabricated in different technologies [65]: in ZMR (Zone Melt Recrystallisation), where an oxide layer is grown on a silicon wafer before a thin layer of amorphous polycrystalline silicon is deposited and crystallised by heating above the melting point; in SIMOX, where the SiO_2 layer is formed by high energy implantation of oxygen into a silicon wafer; in BESOI (Bond and Etch back SOI), where two oxidised silicon wafers with hydrophilic surfaces brought in contact establish weak H-H bonds which are then heated to form a stable bonding and then the surface is thinned by etching to obtain thin film silicon layer for CMOS electronics. The successful implementation of monolithic pixel detectors in SOI technology depends on a careful control of the process parameters,

especially the temperature.

3.3.4 Charge Sensing Element with Built-in Amplification

Charge sensing elements for charged particle detection with a first amplification stage built into the device were proposed in order to increase SNR for monolithic pixel detectors. The idea of built-in amplification is usually based on the internal conversion of the charge, collected in a potential well, to voltage. This conversion takes place on the inner, predominantly parasitic, capacitance of the device. The diffusion regions collecting charge carriers are also used as a substrate for implementing a transistor. The signal amplification is achieved through modulation of the current conveyed via the transistor by a voltage variation on the inner node capacitance. Thus, the device acts as a charge-to-current amplifier. In contrast to the charge-to-current conversion realised in the sensitive element, is the charge-to-voltage conversion performed in Active Pixel Sensors introduced in Chapter 3.3.5. In this case the collected charge melts away between the conversion element and the collection diode. The conversion gain depends on the input capacitance of the conversion element. More rarely, an active processing of currents induced on electrodes, based on the classical charge sensitive amplifier principle, as it is presented in Chapter 3.3.3.2, is used. This results from the usually encountered limitations in the design, where the critical one is that only one type of active element can be implemented within the pixel area.

As a result of having built-in amplification, the detecting element can be made thinner not deteriorating the SNR with respect to the standard, thick device. Stray capacitances due to connections between the sensor and the amplifier are avoided and a very small conversion capacitance can be accomplished.

Two solutions are reported in the literature, where a successful design and operation were experimentally confirmed. Both use indirect charge to current conversion passing through the control electrode whose potential is modified due to the charge collection. The control gate modulates the current in the conductive channel of the dedicated field effect transistor. The current variation is a measure of the collected charge, at the same time the energy deposited by the particle.

A promising device, a p-channel JFET element integrated on a high resisitivity material (DEpleted P-channel FET or DEPFET) was first proposed [66, 67, 68]. Its 300 μm thick

substrate is fully depleted and a potential well is created in the bulk by a sideward depletion and a buried n-type implant into the substrate underneath the transistor channel. The buried n-type implant plays the role of a second internal gate. The electrons liberated as a result of a particle passage are attracted and collected in the internal gate, where they are stored. The collected charge modifies the gate potential resulting in a modulation of the channel current. The operation principle of the annular structure DEPFET device with the source in the centre is shown in Figure 3-14a. The device has non-destructive read-out capability*, but the internal gate gets filled up with signal charges and thermally generated electrons. Thus, it needs clearing, which can be done by biasing a clearing electrode such that the potential well vanishes and the collected charge is transferred to the clearing electrode, from where it is carried away. The read-out is done by applying a measurement current to the device, which is achieved by a proper bias of the top electrode. The DEPFET device addresses very low noise operation manifested in an equivalent charge noise level reported close to $6e^-$ at room temperature. The completion of the pixel with the circuitry to realise some signal processing within the pixel requires great care in order to avoid charge collection by the additional circuitry rather than by the detection element itself. Specialised external VLSI circuits are needed to read-out a DEPFET detector.

Another solution for a monolithic pixel detector with an amplification stage in every pixel is the pMOS pixel device [69, 70]. Figure 3-14b gives a schematic view of a proposed single-sided, two-dimensional read-out device. It is composed of an array of n-wells, which are collecting electrodes. A double-drain pMOS transistor is implanted in each n-well, providing amplification to the detected signal. The drains are ganged together with metal strips in horizontal and vertical directions, providing two-dimensional read-out organised in a strip-like way on a single-sided device. The strip-like configuration keeps the fast read-out advantage of the microstrip detectors, while the subdivision into pixels reduces the detector capacitance and therefore the noise. The detector bias voltage is applied to the backside p^+-type implantation, while the n-well is grounded through a high value bias resistor. The signal charge generated in the substrate is accumulated on the n-well, and decays slowly through the bias resistor. The accumulated charge provides a voltage shift in the n-well, which modulates

* Non-destructive in contrast to destructive read-out, read-out capability means that addressing the cell for read-out its signal does not evacuate the collected charge, preserving it for the possible future read-out.

the drain current of the pMOS device. The resulting differential drain current is then fed into the external preamplifier. For the optimum operation of the device, it is essential to reduce the electronic noise coming from the topside gate of the transistor and to amplify the input signal induced on the backside. This observation leads to a reduction of the front-side transconductance, which was achieved by decreasing the oxide capacitance C_{ox}. The first fabricated prototype of the pMOS pixel presented some limitations: a large detector capacitance, a large leakage current and a poor noise performance. Even though, the initial expectations were not reached a good SNR of 35 and a spatial resolution of 43 μm consistent with the 200-μm pixel pitch were obtained.

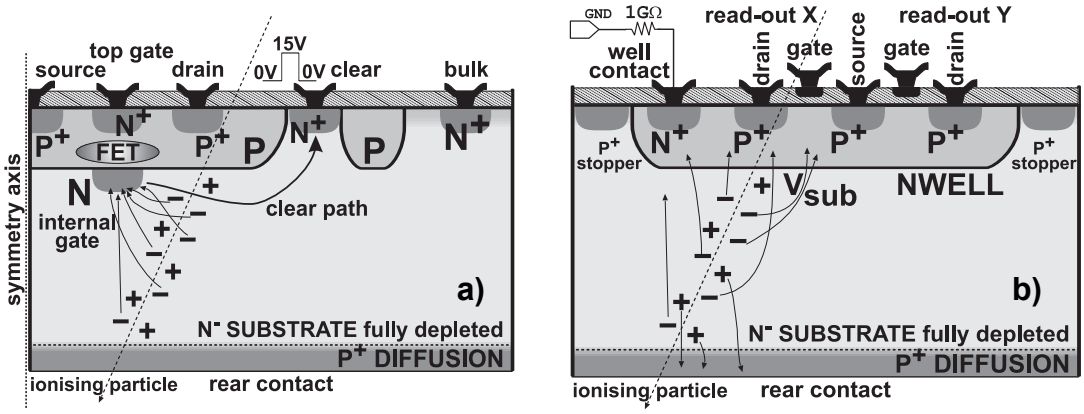

Figure 3-14: (a) Working principle of the DEPFET detector and (b) the pMOS pixel detector.

The principle of the built-in amplification exploited for the pMOS pixel device gave rise to the idea of the double-gate PhotoFET element. The prototype of a new monolithic device for aiming to particle tracking was implemented in a standard CMOS process as it is proposed in Chapter 3.3.5. The principle of a pMOS pixel detector could also be used for a construction of a hybrid device with the first signal amplification located on a detector within each pixel and the further signal processing and readout control implemented on the readout chip. The drain of each pMOS device would be connected to the dedicated read-out channel in this case by means of a bump bonding technique.

3.3.5 Monolithic Active Pixels Sensors in a Standard CMOS Process

Monolithic Active Pixel Sensors (MAPS) constitute a novel technique for silicon position

sensitive detectors. The sensors are fabricated in a standard CMOS process used for modern integrated circuits manufacturing. The details about the processes, physics device simulations, design aspects as well as the results obtained in extended tests with emphasis on tests with a radioactive source and high energy charged particles beams are given in the following sections. The baseline architecture of the proposed device is similar to a visible light CMOS camera, emerging recently as a substantial competitor to standard CCDs for digital photography and video applications [71].

The new element, distinguishing MAPS from classical detectors on a fully depleted, high resistivity substrate, is the charge collection achieved from a lightly doped undepleted epitaxial layer used as the active volume. The development of MAPS for particle physics applications was inspired by the use of this technique in visible light applications. In this domain, the use of epitaxial layer has proven its effectiveness by reducing the pixel blind area to the metal lines absorbing the visible light [72]. The first MAPS prototype structures aiming to charged particle detection named MIMOSA* were fabricated in 1999 [73, 74, 75] and their functionality was successfully tested The measured tracking performance of minimum ionising particles includes very high spatial resolution of 1.5 μm and the detection efficiency close to 100%, resulting from a high signal to noise ratio of more than 30 [76, 77, 78].

The signal sensed in the MAPS detector has a form of weak and short in time current pulses induced on pixel electrodes. The current is induced on some number of the adjacent pixels, which are closest to the particle impact point. The current is integrated on a collection diode producing a voltage drop whose magnitude depends on the distance between a given pixel and the impact point. The total amount of charge available from a single event depends on the thickness of the epitaxial layer. The charge liberated in the highly doped substrate, on which the epitaxial layer is grown, is mostly lost due to fast recombination of carriers. However, some fraction of this charge diffusing from the substrate to the epitaxial layer can still be collected. The design and fabrication of MAPS follows the developments in microelectronic industry. The current trends, related to scaling down the technology feature size, are to reduce also the thickness of the epitaxial layer†. This translates into less charge,

* MIMOSA stands for **M**inimum **I**onising Particle **MOS A**ctive Pixel Sensor.

† Thinner epitaxial layer improves the immunity of the electronics to interferences, latch-ups and the parasitic couplings between different components on the same substrate.

which can be collected but is particularly compensated by the good noise performance.

The epitaxial layer is available in numerous modern CMOS VLSI processes, featuring twin tubs, where it is grown on a highly, usually p^{++}-type doped substrate. The principle of this new structure is sketched in Figure 3-15. This figure shows the cross section through the wafer sandwich-like structure composed of the substrate, the epitaxial layer and the p-well. The pixel level read-out electronics is placed in the p-well. Another information in this figure is the distribution of the electric potential with its minimum in the region of the n-well. Since, there is no strong electric field, the charge carriers, generated after the impact, diffuse at thermal velocities towards the collecting diodes.

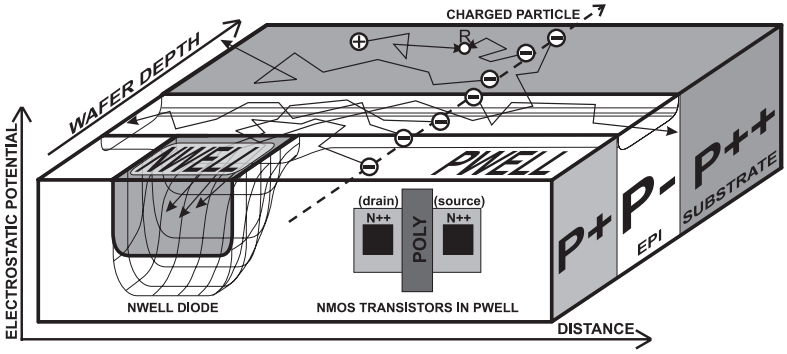

Figure 3-15: Sketch of the structure of MAPS for charged particle tracking. The charge-collecting element is an n-well diode on the p-type epitaxial layer. Because of the difference in doping levels (about three orders of magnitude), the p-well and the p^{++} substrate act as reflective barriers. The generated electrons are collected by the n-well/p-epitaxial diode.

In the new device, the charge generated by the traversing particle is collected by the n-well/p-epitaxial diode, created by the floating n-well implantation reaching the epitaxial layer. This structure forms a potential well that attracts electrons. The active volume, i.e. epitaxial layer, is underneath the readout electronics allowing a 100% fill factor, as required in tracking applications. Depending on the capacitance of the charge-collecting element, this typically yields less than 20 mV of the total signal per MIP. One limitation of the proposed approach is the limitation of the design at the pixel level to NMOS transistors only, whereas both types of transistors are used at the chip periphery. This results from the use of n-well implantation areas for the collecting diodes.

The basic single cell read-out architecture of a MAPS detector is shown in Figure 3-16. The transistor M1 resets the diode to the reverse bias, the transistor M3 is a row switch, and

while the transistor M2 constitutes one part of the source follower. The current source for the source follower and the column selection switch are located outside the pixel. Such a pixel configuration provides capability of continuous charge integration within time between two consecutive reset operations.

The small size of a single pixel, which contains in the basic configuration only the charge collecting diode and three transistors used for signal read-out, allows assembling active arrays with a tight read-out pitch of 20 μm or less. After noise optimisation, taking into account the actual working conditions i.e. read-out frequency and single pixel sampling, equivalent noise charges of below 10 e^- are achievable even for operation at room temperature. The compact layout in combination with the measured high SNR results in a very good spatial resolution as required by new high-energy physics experiments.

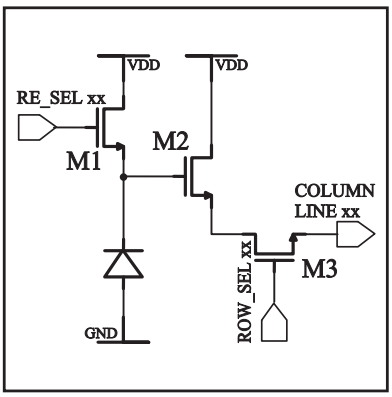

Figure 3-16: The basic single cell read-out architecture of a CMOS MAPS detector.

The device can also eventually be thinned down to very small thickness in order to reduce multiple scattering. Thus, the MAPS detectors provide a thin, and precise tracking device for a future e^+e^- linear collider. In this application, the signal accumulation over a number of bunch crossings is a straightforward mode of operation for the MAPS devices. Another important characteristic of the MAPS detectors is low power operation, which is achieved by the activation of the circuitry in each pixel only during the read-out and, contrary to CCDs, there is no power dissipation due to high frequency clock signals driving large capacitances. The major advantage of MAPS detectors is the fabrication process. Unlike the previously proposed monolithic tracking devices, the new device can be fabricated using a standard, cost effective and easily available CMOS process. Four small scale prototype chips,

which have been fabricated using 0.6 μm 0.35 μm with and without epitaxial layer and a 0.25 μm CMOS processes, validated the concept of this approach. The small prototype chips designed as arrays of 64×64 and 128×128 square pixel elements were equipped with a serial analogue readout, requiring only two digital signals to operate. Such a simple read-out arrangement allowed easy operation of the device and was sufficient for demonstrating the feasibility of the new detection technique.

The detectors for future High Energy Physics experiments must be optimised for physics performance, taking consideration of the specific environment of the accelerating machine The future linear collider physics experiments are supposed to deal with signals occurring at limited events rates and reach in secondary vertices, which implies optimal vertex detection. The MAPS detectors presented in this work have been proposed in the context of developing a new detector technology capable to fulfil requirements put on the construction of the vertex detector at a future linear collider [79]. The development was driven particularly by a potential application at the TESLA experiment [80]. The MAPS detectors are one of three technology options currently considered for the vertex detector construction at this experiment. The alternative design technologies are based on CCDs, for which most of the practical experience dated back to the SLD application exists, and the hybrid pixel sensors. The detailed description of the environment, design constraints and requirements to be met at TESLA are given in Chapter 1.4. Fulfilling these conditions defines guidelines for the vertex detector, which should be optimised specifically for the operation in an untriggered, continual and dead-timeless read-out mode with strict constraints laid down on the minimised power consumption. The preliminary estimation of the background and the required vertexing precision lead to the pixel size of approximately $20 \times 20\ \mu m^2$, a typical read-out time in the order of 100 μs with the 20 μs option for the first layer and the ladder thickness reduced to about 50 μm. The vertex detector will be exposed to irradiation in the order of 100 krad of the ionising dose and the fluence of 1 MeV neutron equivalent close to 5×10^9 n/cm^2 integrated over 5 years of the experiment lifetime.

Chapter 4

SIMULATIONS OF CHARGE COLLECTION IN MAPS DEVICES

4.1 Introduction

An important tool in the design of MAPS for charged particle tracking is the physics simulation of the device. There are two motivations for this kind of simulations. In the first place, they are needed in order to achieve a quantitative estimation of the charge collection properties including charge collection efficiency and spatial charge spreading onto the neighbouring pixels. The precise track determination by application of a centroid finding method is in principle very attractive for a detector made with undepleted epitaxial material, where the charge sharing mechanism is efficient and the high SNR is provided. Secondly, they are also important to understand better the charge collection mechanism and its time properties. The amount of collected charge and the collection time depend on the geometry and the electrical properties of the detector. The important construction parameters are the active layer thickness, the size of a pixel and of the collecting diode and also their mutual arrangements. The choice of some of these geometrical parameters is up to the designer, while the epitaxial layer thickness and doping profiles are defined for a given fabrication process and cannot be changed by the user. The device simulation guides the designer in the choice of the process and of detector geometry. The active part of the MAPS is mainly limited to the relatively thin almost undepleted epitaxial layer, where the minority carrier lifetime is long enough with respect to the collection time. The best expected signal is about 1000 electrons for the CMOS fabrication processes offering the thickest epitaxial layers.

The market of software tools for semiconductor device simulation at the physical level is narrow, and only a limited number of products are available. Most of them allow 2-D modelling, and the few that can work in 3-D often offer insufficient simulation precision.

The device modelling oriented towards 2-D representation has a limited value for pixel detectors, which are intrinsically 3-D devices. Only 3-D simulations allow to model the detector operation in a rigorous manner without simplification of the geometry. Precise models are of crucial importance for the analysis of the device performances. Moreover,

some flexibility in device description and the possibility to use adequate built-in models of properties like carrier mobility, carrier recombination and transport mechanisms, external magnetic field and temperature dependence are very important. This motivates the use of an advanced tool for technological process analysis. The commercial ISE-TCAD package by ISE AG [81] fulfils most of the aforementioned requirements and was therefore chosen.

4.2 Simulation of Charge Collection

4.2.1 Simulation Tool

This paragraph gives a detailed description of ISE-TCAD. In ISE-TCAD values of the collected charge are obtained by a straightforward integration of the contact currents, while the charge collection process results from achieving the equilibrium state after excitation by the ionising particle.

4.2.1.1 Electric Device Model

The "drift-diffusion" transport model [81], used to study the charge collection mechanism, makes use of only three independent variables: ψ, n and p, which are the electrostatic potential and the electron and hole concentrations, respectively. The three governing equations in this model are the Poisson equation and the two continuity equations for the electron and hole densities. The Poisson equation relates variations in the electrostatic potential to the local charge densities. The continuity equations describe how the electron and hole densities evolve as a result of transient transport, generation and recombination processes. The Poisson equation is given by

$$\varepsilon_{si}\nabla^2\psi = -q\left(p - n + N_D{}^+ - N_A{}^+\right), \tag{4-1}$$

where ε_{Si} is the electric permittivity of silicon and $N_D{}^+$, $N_A{}^-$ are the concentrations of ionised donors and acceptors, respectively. In present CMOS processes, boron and phosphor atoms are normally used as donors and acceptors. Their impurity levels in silicon are sufficiently shallow, justifying the assumptions of the complete dopants ionisation model at room temperature. The density of charge created in any part of the detector by an impinging particle is negligible compared to the density of ionised atoms of impurities at room temperature. Therefore, the potential distribution in the detector volume can be calculated by

taking into account only the distributions of thermally created charges and ionised impurities and externally applied voltages to the contact electrodes. Then, the constant electric field can be assumed for the charge transport. The continuity equations for electrons and holes are

$$\nabla \overrightarrow{J_n} = qR + q\frac{\partial n}{\partial t} \quad \text{and} \quad \nabla \overrightarrow{J_p} = qR + q\frac{\partial p}{\partial t}, \tag{4-2}$$

where R is the net rate of electron-hole recombination and the vectors $\overrightarrow{J_n}$ and $\overrightarrow{J_p}$ are the electron and hole current densities expressed as

$$\overrightarrow{J_n} = -nq\mu_n \nabla \varphi_n \quad \text{and} \quad \overrightarrow{J_p} = pq\mu_p \nabla \varphi_p . \tag{4-3}$$

Here, μ_n and μ_p are the electron and hole mobilities, and φ_n, φ_p are the electron and hole quasi-Fermi potential. The quasi-Fermi levels are introduced to relate the carrier density to the electrostatic potential for non-equilibrium conditions. This allows computing the electron and hole densities using the following formulas

$$n = N_c e^{\left(\frac{q\varphi_n - E_c}{kT}\right)} \quad \text{and} \quad p = N_v e^{\left(\frac{E_v - q\varphi_p}{kT}\right)}, \tag{4-4}$$

where E_c and E_v stand for the conduction and valence band energy edges, respectively and consequently N_c and N_v are the effective densities of states in the conduction and the valence band. The quantities, N_c and N_v, are defined by

$$N_c = 2\left(\frac{2\pi m_e kT}{h^2}\right)^{3/2} \quad \text{and} \quad N_v = 2\left(\frac{2\pi m_h kT}{h^2}\right)^{3/2}, \tag{4-5}$$

with m_e and m_h denoting the effective mass of the electron and the hole, respectively. Evaluation of (4-5) yields the values for the effective densities of states $N_v = 1.04 \times 10^{19} \times (T/300)^{(3/2)}$ cm^{-3} and $N_c = 2.8 \times 10^{19} \times (T/300)^{(3/2)}$ cm^{-3}. Relating the conduction and valence band energy edges to the electrostatic potential, the quasi-Fermi potentials are given by

$$\varphi_n = \psi - \frac{kT}{q}\ln\left(\frac{n}{n_{i,eff}}\right) \quad \text{and} \quad \varphi_p = \psi + \frac{kT}{q}\ln\left(\frac{p}{n_{i,eff}}\right), \tag{4-6}$$

where $n_{i,eff}$ is the effective intrinsic carrier density accounting for the effect of band gap narrowing.

The correspondence of (4-3) and the conventional formulation of "drift-diffusion" for conduction electrons, given by

$$J_n = nq\mu_n \vec{E} + qD_n \nabla n, \tag{4-7}$$

is established if

$$D_n = \frac{kT}{q}\mu_n, \tag{4-8}$$

i.e. if the Einstein relation holds for a temperature equal to the lattice temperature. The effective intrinsic carrier density, $n_{i,eff}$, is an increasing function of temperature and is defined as

$$n_{i,eff} = n_i \gamma_{BGN} \quad \text{with} \quad n_i = \sqrt{N_c N_v} e^{\left(-\frac{E_g}{2kT}\right)} \quad \text{and} \quad \gamma_{BGN} = e^{\left(-\frac{\Delta E_g}{2kT}\right)}, \tag{4-9}$$

where ΔE_g stands for the band gap narrowing effect. The intrinsic carrier density of undoped silicon, n_i =1.45 × 10^{10} cm^{-3}, at room temperature T=300 K.

An appropriate set of dependencies and physics models, including all the important parameters for the charge transport through thermal diffusion in the epitaxial layer and charge collection mechanism by n-well/p-epi diodes, was chosen. The doping dependent mobility of charge carriers was modelled according to the Massetti model [82]. It takes into account scattering of the carriers with the charged impurities in the doped semiconductor, which leads to degradation of the carrier mobility [81]. The effect was modelled by the expression for the carrier mobility, μ_{dop}, written as

$$\mu_{dop}(N_i) = \mu_{min1} e^{\left(-\frac{P_c}{N_i}\right)} + \frac{\mu_{const} - \mu_{min2}}{1 + \left(\frac{N_i}{C_r}\right)^{\alpha}} - \frac{\mu_1}{1 + \left(\frac{C_s}{N_i}\right)^{\beta}} \quad \text{and} \quad \mu_{const} = \mu_L \left(\frac{T}{T_0}\right)^{-\varsigma}, \tag{4-10}$$

where $N_i = N_D^+ + N_D^-$ denotes the total concentration of the ionised donor and acceptor impurities. The values for the reference mobilities, μ_{min1}, μ_{min2} and μ_1, as well as the reference doping concentrations, P_c, C_r and C_s, and the exponents, α and β, are given in Table 4-7. The parameter μ_L is the intrinsic (low-doping) reference carrier mobility accounting only for lattice vibrations. The bulk-phonon scattering gives rise to a mobility, which falls rapidly as the lattice temperature T increases. The temperature T_0 in (4-10) is the reference temperature equal to 300 K.

Table 4-7: Parameters for the doping dependent Masetti mobility model.

Model parameter	Electrons	Holes	Units
μ_{min1}	52.2	44.9	$cm^2/(Vs)$
μ_{min2}	52.2	0	$cm^2/(Vs)$
μ_1	43.4	29.0	$cm^2/(Vs)$
P_c	0	9.23×10^{16}	cm^{-3}
C_r	9.68×10^{16}	2.23×10^{17}	cm^{-3}
C_s	3.34×10^{20}	6.10×10^{20}	cm^{-3}
α	0.68	0.719	-
β	2.0	2.0	-
μ_L	1417.0	470.5	$cm^2/(Vs)$
ς	2.5	2.2	-

For the net recombination rate, required in the drift-diffusion model, only the contribution due to the recombination via deep levels in the band gap, usually called Schockley-Read-Hall (SRH) mechanism [82], was taken into account. According to this model the recombination rate R^{SRH} is expressed by the following formula

$$R^{SRH} = \frac{np - n_{i,eff}^2}{\tau_p (n + n_1) + \tau_n (p + p_1)} \quad \text{with} \quad n_1 = n_{i,eff} e^{\frac{E_{trap}}{kT}} \quad \text{and} \quad p_1 = n_{i,eff} e^{-\frac{E_{trap}}{kT}}, \quad (4\text{-}11)$$

where $n_{i,eff}$ is the effective intrinsic carrier density and E_{trap} is the difference between the defect energy level and the intrinsic level. However, the knowledge on material properties, which is basically available only through precise measurements, was not sufficient to provide correct values for the defect levels into the simulation program*. Thus, the default value for the parameter, E_{trap}=0, was assumed, possibly overestimating the values of carrier lifetimes. The minority SRH carrier lifetime τ_{dop} dependence on the doping concentration was determined by the Sharfetter relation [81]

$$\tau_{dop}(N_i) = \tau_{min} + (\tau_{max} - \tau_{min}) \left[1 + \left(\frac{N_i}{N_{ref,\tau}} \right) \right]^{-\gamma}, \quad (4\text{-}12)$$

* The detailed information on fabrication process parameters, including properties of processed materials, is not usually eagerly provided by silicon foundries. Eventual measurements are difficult due to complex structure of the fabricated devices, usually small die size and restricted regulation concerning reverse engineering techniques.

where the default values used for the reference carrier lifetimes, τ_{min} and τ_{max}, as well as the reference concentration of ionised impurities, $N_{ref,\tau}$, and the exponent γ are summarised in Table 4-8. The carrier lifetime dependence on temperature was modelled according to a power law

$$\tau(T) = \infty \left(\frac{T}{T_0} \right)^{\alpha}, \tag{4-13}$$

where the exponent α equals $-3/2$. This results in the carrier lifetime τ combined dependence on the doping concentration and the temperature, given by

$$\tau(T, N_i) = \tau_{dop}(N_i) \left(\frac{T}{T_0} \right)^{-3/2}. \tag{4-14}$$

The electron and hole diffusion lengths in p-type and n-type silicon, L_e and L_h, respectively are related to the electron and hole lifetimes, τ_e and τ_h, and the electron and hole mobility, μ_e and μ_h, through the equations

$$L_e = \sqrt{\frac{kT}{q} \mu_e \tau_e} \quad \text{and} \quad L_h = \sqrt{\frac{kT}{q} \mu_h \tau_h}. \tag{4-15}$$

The diffusion length determines an average distance at which a minority carrier with a specific lifetime can be found from the point where it was generated. The diffusion length is as good as the carrier lifetime a measure of the dynamics of the system. Switching from one to the other via the Einstein relation is always possible.

Table 4-8: Parameters for the doping dependent Scharfetter SRH lifetimes model.

Model parameter	Electrons	Holes	Units
τ_{min}	0	0	s
τ_{max}	1.0×10^{-5}	3.0×10^{-6}	s
N_{ref}	1.0×10^{16}	1.0×10^{16}	cm^{-3}
γ	1	1	-

The value of the band gap depends on lattice temperature as well as on concentration of impurities. The band gap dependence resulting from doping concentration was based on the so-called Slotboom *Apparent Gap-Narrowing* model [81]. The Slotboom model was basically

developed for p-type materials, but it can equally be used for n-type materials by appropriately setting its parameters. The band gap narrowing effect is described by the following empirical formula

$$\Delta E_g(N) = \Delta E_{g0} + E_{BGN}\left[\ln\frac{N_{A,D}}{N_{ref,\Delta E_g}} + \sqrt{\left(\ln\frac{N_{A,D}}{N_{ref,\Delta E_g}}\right)^2 + 0.5}\right], \quad (4\text{-}16)$$

where ΔE_{g0} =-4.795 × 10^{-3} eV, E_{BGN} =6.92 × 10^{-3} eV, and $N_{ref,\Delta E_g}$ =1.3 × 10^{17} cm^{-3} and $N_{A,D}$ is the donor or acceptor doping concentration used according to the material type. The value of the energy band gap is calculated combining both doping and temperature dependences, according to the following formula

$$E_g = E_{g0} + \Delta E_g(N) + \Delta E_g(T) \quad \text{with} \quad \Delta E_g(T) \approx -\frac{\alpha_{E_g} T^2}{\beta_{E_g} + T}, \quad (4\text{-}17)$$

with α_{E_g} =4.73 × 10^{-4} eV/K and β_{E_g} =6.36 × 10^{2} K.

Each simulation was carried out in three main steps. In a first step only the static solution of the Poisson equation was found. This leads to the distribution of the electrostatic potential within the simulated structure. Following this step, the static solution to the coupled Poisson and continuity equations was computed, where the solution from the first step was used as a starting point for the iteration process in the second step. In the third step the transient simulation was started. The electrode currents due to carrier excitation into the conduction band by the particle passage were calculated. The excess charge was defined at the beginning of the transient simulation according to the predefined ionisation rate emulating the interaction of the charged particle with the detector material. Only the solution of the electron continuity equation was computed during the transient simulation. The previously calculated potential distribution and hole currents were used as the steady state solution, and they were not updated during the transient simulation. This approach was motivated by two facts. Firstly, the density of the charge created in any part of the detector is negligible compared to the density of the ionised atoms of impurities at room temperature. Thus, the electrostatic potential distribution is barely affected by the moving carriers. Secondly, because of the specific design of the detector, the holes are prevented from giving their contribution to the total collected charge.

4.2.1.2 Generation of Charge Carriers

In the simulations, DESSIS-ISE was used to solve the semiconductor device equations for the "drift-diffusion" carrier transport model in three dimensions. The charge distribution, simulating particle interaction with the detector, was declared at the beginning of each transient simulation. The impact position defined as a point on the detector surface and the distribution of the generated charge density along the particle track were specified. The magnitude of excess charge was closely adapted to reflect real charge clouds due to the way in which simulated particles interact. Two models of excess charge generation, which are available in the ISE-TCAD, were adapted by optimising the choice of their parameters to simulate minimum ionising particles and X-ray photons.

The *alpha-particle* model, available for transient simulations, was used to describe the excess charge due to a single passage of a minimum ionising particle. A uniform charge distribution along the particle track with a characteristic value of 76 e-h pairs for each micrometer of the track was assumed. The radial charge distribution was declared gaussian with a constant width along the particle track of $\sigma = 0.75$ μm.

The *heavy-ion* model, available also for transient simulations with DESSIS-ISE, was used to generate excess charge carriers in the detector due to a single impact of X-ray photons. The charge, in this case, was generated as a cloud centred on assumed interaction point. The radial charge distribution in the cloud was declared gaussian with a width $\sigma = 1.0$ μm. The amount of generated charge in each single interaction was determined as a ratio of the photon energy and the average energy needed to create an e-h pair W=3.6 eV. The *heavy-ion* model was particularly used to validate the method of charge-to-voltage gain calibration exploiting low-energy X-ray photons, as shown in Chapter 5.3.3.

The detailed descriptions of both models with complete lists of parameters used in simulation are given in Appendix-B.

4.2.2 Detector Geometry

The device geometry, as described by a mesh produced from the boundary definition and doping information by the 3-D mesh generating program, MESH-ISE, was examined by DESSIS-ISE. The DESSIS-ISE tool is a multidimensional, mixed mode device and circuit simulator. The simulated structure was described by the boundary inside which the mesh and

doping profiles were defined. The mesh granularity volume was adjusted in some critical parts of the detector to gradients of the doping concentrations, the density of injected excess charge and the demanded computation precision. The mesh was much more refined in those regions, which featured, increased electric field or increased gradients of either doping concentrations or carrier densities. In this way, the operation of the detector could be modelled in an accurate way without significant simplification of its geometry. The structure modelled two complementary doping wells implanted into a thin, relatively high resistive (~10 Ωcm) and an epitaxial layer deposited on a heavily doped p-type substrate (~0.1 Ωcm). The doping information used in simulations was based on the profiles provided by the VLSI foundry for an existing twin-tub CMOS 0.6 μm process. The profiles, presented in Figure 4-1a, can be considered as typical for a whole family of modern, twin-tub bulk CMOS processes. The two curves in this figure ($n^{++}/n^{+}/p^{-}/p^{++}$) and ($p^{+}/p^{-}/p^{++}$) sample the doping concentration along a line passing through the collecting diode and through the p-well, respectively. Figure 4-1b shows the corresponding profile of the electron lifetime resulting from doping dependence determined according to the model described in Chapter 4.2.1.1.

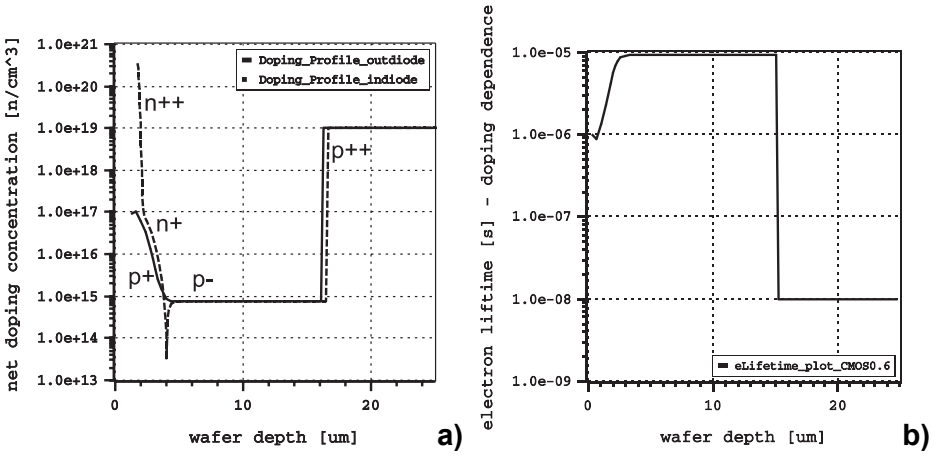

Figure 4-1: (a) Doping profiles, used in the detector simulations, as a function of the wafer depth, (b) electron lifetime profile resulting from doping dependence.

The lifetime information is plotted as a function of distance from the device surface, traversing the p-well, epitaxial layer and the substrate. The boundary and command input files for MESH-ISE were prepared for two arrangements of charge collecting diodes within a pixel cell of $20 \times 20\ \mu m^2$. The first configuration comprised a single diode and the second one featured four diodes connected in parallel and shortened to a separate node. The surface

of a single diode was fixed at $3 \times 3\ \mu m^2$ with its depth being determined by the doping profile. The main geometrical parameters of the detector structures studied in the simulation are summarised in Table 4-9.

Table 4-9: Geometrical detector parameters for simulation.

Simulation Parameter	
Single pixel size	x=20 μm, y=20 μm
Number of diodes per pixel	one, four
Diode size	$3 \times 3 \times \sim 2.5\ \mu m^3$
Diodes position	symmetric within pixel
Substrate thickness	0 μm, 15 μm
Epitaxial layer thickness	5 μm, 15 μm, 25 μm
Max size of simulated structure size	3 × 3 pixels

At the first step, the boundary and command files for MESH-ISE were prepared by means of the layout editor program, PROLYT-ISE, and the process simulator, PROSIT-ISE. The physical mask describing the pixel layout was imported directly from the CADENCE* layout editor passing through the CIF† format. The simplified description of the process flow, resulting in demanded doping profiles, was prepared under PROSIT-ISE and used to automate MESH-ISE input files generation. At the second approach the input files were parameterised, allowing the user an easy selection of the simulated structure configuration. As simulation parameters, the following quantities were specified: both orthogonal pixel dimensions, the number of diodes, their size and position within the pixel area, the epitaxial and substrate layer thickness and the position of an impinging particle.

The epitaxial layer thickness is a characteristic feature of a given process. The active volume of the detector is mostly limited to this layer, since most of the collected charge originates in it. The epitaxial layer thickness is irrefutably considered as a key criterion for choosing the particular process for MAPS fabrication. The epitaxial layer thickness was parameterised and simulations were performed for three different values of it: 5 μm, 15 μm and 25 μm. The mesh refinement, optimised in terms of computation time and the required precision of analyses, was defined different in each part of the device. The finest mesh size, i.e. 1 μm, 1 μm, and 1.5 μm (1, 1, 1.5), respectively, along both horizontal axes and the vertical direction, was defined only in the volume underneath the pixel whose surface was traversed

* CADENCE name of the software environment for integrated circuit design.

† CIF the database format for layout representation of integrated circuits (Caltech Interchange Format).

by the particle track. The pixel directly touched by the particle is called *the central pixel* for further reference. For the eight adjacent neighbours of the central pixel, the maximum allowed mesh size was defined (2, 2, 2) and was increased to (3, 3, 3) within the additional volume outside the cluster of 3×3 pixels. In the areas of sudden changes of doping concentrations, which were located close to and inside the collecting diodes, the mesh size was reduced to (0.5, 0.5, 0.5). Additionally, the mesh density in the cubic volume of the base surface $3 \times 3\ \mu m^2$ around the particle track was restricted to (0.25, 0.25, 0.25). The maximum simulated volume of the detector structure was $122 \times 122 \times 45\ \mu m^3$, filled with a generated mesh of up to 0.25×10^6 vertices*. The number of mesh vertices depended on the thickness of the simulated structure and it was optimised between the required accuracy and the calculation speed. An example of a 3-D mesh used for the 3×3 pixels cluster is shown in Figure 4-2. The actual 3×3 pixels cluster constitutes only 25% of the simulated entity.

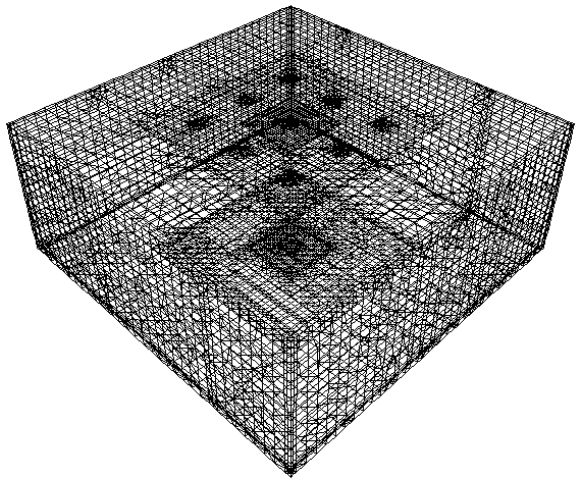

Figure 4-2: Example of the 3-D mesh used for the cluster of 3×3 pixels in the case of the single-diode pixel configuration.

The device boundaries in DESSIS-ISE can only be treated with the reflective boundary conditions†, which potentially leads to the overestimated signals due to ghost carriers reaching the boundary. In the real device, charge carriers diffusing far away from the impact point are

* The upper limit in number of mesh vertices results from the limited capacity (mainly still due to not sufficient RAM memory) of the computer used for performing transient simulations with DESSIS-ISE. One complete simulation, devoted to a single particle passage, took around one hours for mesh and up to ten hours of transient simulation (PC under LINUX, PIII, 850 MHz, 1.5 GB of RAM and 1 GB of disk swap).

† Reflective boundary conditions (called also ideal Neumann) for drift-diffusion model used for analysing the device can be expressed as: $\vec{E} \cdot \vec{S_n} = 0$, $\vec{J_n} \cdot \vec{S_n} = 0$, $\vec{J_p} \cdot \vec{S_n} = 0$ - where $\vec{E}$ is a vector of the electric field, $\vec{J_n}$ and $\vec{J_p}$ are electron and current densities, respectively and $\vec{S_n}$ is a unity-length vector normal to the boundary surface.

either collected by other diodes or they recombine in the detector volume. The relatively large part of dummy silicon was added outside the cluster volume in order to emulate with the highest possible efficiency non-reflective boundary conditions. Additionally, in order to better emulate the real situation of the a priori unlimited charge spreading, the electrons diffusing close to the defined device boundaries "were eaten up" by the artificially high recombination velocity declared at these regions. This effect was achieved by adding four belts, about 1 μm thick, surrounding laterally the whole detector volume. Owing to the fast recombination at the created interface regions, the electrons were prevented from being reflected backwards. In this way the effect of the reflective boundary conditions was efficiently suppressed.

4.2.3 Charge Collection Simulation Results

The first step in the charge collection simulations was to determine the electric field and the electric potential inside the detector of the particular geometrical configuration under examination. An example of these computations is shown in Figure 4-3. The electric field and the electric potential are almost zero in the whole detector volume. As opposed, the close vicinity of the n-well implantations forming collecting diodes is the only place with a strong electric field. The potential drops in these places allowing electrons to be extracted from the epitaxial layer. The collected charge is sensed as a voltage drop on the n-well/p-epi junction capacitances, which is then transferred to the readout electronics. Some electric field, however very weak, is present also at both borders of the epitaxial layer, from one side at the substrate and on the other side at the p-well interfaces. The depletion zone of the reverse polarised n-well/p-epi diodes, W_{depl}, is very shallow. Its thickness is approximated from the formula valid for the abrupt-type junction

$$W_{depl} = \sqrt{\frac{2\varepsilon_{Si}}{q}\left(\frac{N_{A,p-epi} + N_{D,n-well}}{N_{A,p-epi}N_{D,n-well}}\right)\left(V_{bi} - V_R\right)}\ , \qquad \text{with} \quad V_{bi} = \frac{kT}{q}\ln\left(\frac{N_{A,p-epi}N_{D,n-well}}{n_i^2}\right) \qquad (4\text{-}18)$$

where $N_{A,p-epi}$ and $N_{D,n-well}$ are the acceptor-type and donor type doping concentrations in the epitaxial layer and in the p-well region, respectively and V_R is the reverse bias voltage on the diode. The achievable value of the voltage, V_R, and dopant densities vary for different

processes. The estimated thickness of the depletion zone is below 2 μm for the typical reverse bias of 3.2 V. Small potential barriers, $V_{bar,sub}$ and $V_{bar,pwell}$, present at the interfaces to the epitaxial layer with the substrate and the p-well region, respectively, are given by

$$V_{bar,sub} = \frac{kT}{q}\ln\left(\frac{N_{A,p-sub}}{N_{A,p-epi}}\right) \quad \text{and} \quad V_{bar,pwell} = \frac{kT}{q}\ln\left(\frac{N_{A,p-pwell}}{N_{A,p-epi}}\right), \tag{4-19}$$

where $N_{A,p-sub}$ and $N_{A,p-pwell}$ are the acceptor-type doping levels in the substrate and in the p-well region.

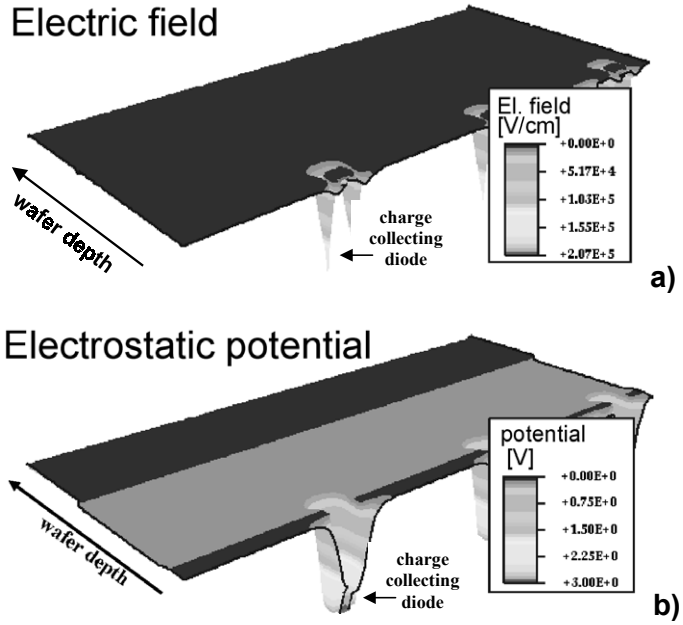

Figure 4-3: (a) Projection of the electric field and (b) the potential in the detector.

The electrons generated in the undepleted epitaxial layer can diffuse in all directions. However, those, which approach the interfaces with the substrate and with the p-well region, are reflected by the field back into the epitaxial layer. For doping profiles depicted in Figure 4-1, the potential barriers are calculated $V_{bar,sub}$ =245 mV and $V_{bar,pwell}$ =125 mV. Bearing in mind the thermal potential $kT/q \approx 25.6$ mV at 300 K, both interfaces act as perfect mirrors for electrons, which diffuse at thermal velocities. The electrons continue diffusing in the epitaxial layer until they happen to approach the p-n junction of the n-well/p-epi diode at which point they start feeling the electric field. The electrons are promptly transported by the electric field and then are stored on the junction capacitance. These electrons, which originate

in a highly doped substrate, are mostly lost by fast recombination. The ionising particle traversing the detector leaves usually charge on some number of collecting diodes forming a cluster of several pixels. The width of the cluster is related to the epitaxial layer thickness and the diodes arrangement. An example of a transient simulation is presented in Figure 4-4. The case, which is shown, illustrates a particle hitting within the central pixel of the cluster and passing directly through the collecting diode. The electron concentrations in two transient simulation steps, i.e. at the impact time and 25 ns later, are depicted on the three dimensional cross-sections (cut-plane) of the detector structure. The charge in the epitaxial layer spreads more rapidly and vanishes slower than in the substrate. This effect results from the increased recombination velocity and the decreased mobility of electrons in the substrate, where the doping level is higher.

The crucial parameter for the charge collection is the carrier lifetime in the epitaxial layer, in the p-well and in the substrate. The lifetimes for non-irradiated materials depend mainly on doping concentrations and the material quality like bulk defects and charge traps. The latter is unknown, and was not included into simulations. The doping dependence based on the empirical relation (4-12) yields electron lifetimes* of 10 ns in the substrate, 10 μs in the epitaxial layer and between 1 μs and 10 μs in the p-well. For each combination of parameters given in Table 4-9, including the thickness of the epitaxial layer, the number of diodes per pixel and the thickness of the substrate, 33 separate transient simulations were performed. Each treated a single event of an ionising particle at fixed impact point. Two characteristic parameters, i.e. the charge collection efficiency and the collection time, were determined for each step. The impact positions were chosen randomly using the *Design-of-Experience* (DOE) option available when running the GENESIS-ISE environment [81]. The spatial distribution of chosen impact points is shown. The simulations were carried out for two pixel designs, i.e. with one and four parallel diodes. The numbers, placed in Figure 4-5 next to the symbol for each position of the impinging particle, stand for the amount of the collected charge within the central pixel. The collected charge is given in number of collected electrons for the 15 μm thick epitaxial layers. For the convenience, the resolution used for presenting particle impact points in this plot is 1 μm. This explains why two different points with seemingly

* The electron properties can be also specified by diffusion length. One finds $L_e = \sim 0.17 \times 10^{-3}$ cm, $\sim 19 \times 10^{-3}$ cm and $\sim 4.5 \times 10^{-3}$ cm in the substrate, epitaxial layer and in the p-well, respectively.

symmetrical location within the pixel area yield different number of collected charges.

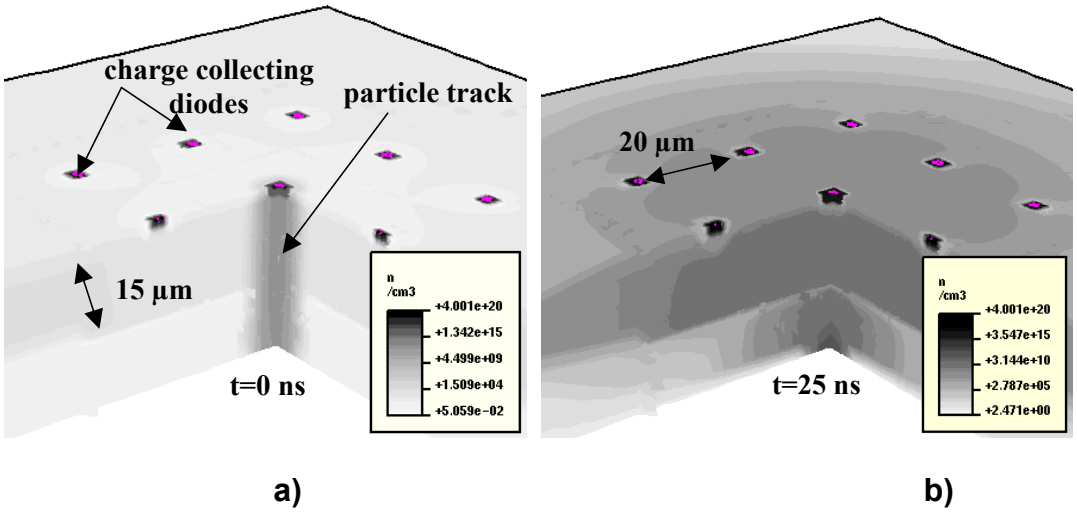

Figure 4-4: Charge spreading for one example of the simulated particle impact – central hit for a pixel configuration with a single diode. (a) Electron concentration at the impact time and (b) 25 ns later.

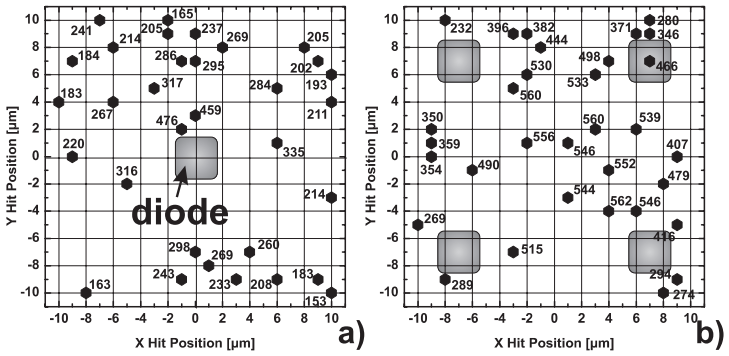

Figure 4-5: Simulated particle impact positions restricted to the area of the central pixel and corresponding numbers of electrons collected on the central pixel for (a) single-diode and (b) four-diode pixel configurations for the 15 µm thick epitaxial layer.

The charge collection efficiency and the collection time were analysed for three different cluster sizes, i.e. single cell, 2 × 2 and 3 × 3 pixels, and varying the distance between the impact position and the middle point of the collecting diode in the central pixel. Selected results are presented in Figure 4-6 and Figure 4-7. They were obtained for an epitaxial layer thickness of 15 µm and pixel designs with a single diode or four parallel diodes. The currents and magnitude of the collected charge on the central pixel and on its three selected closest neighbours are plotted as a function of time after the particle impact. The collected charge was determined by integration of the currents passing through the contact electrodes which

were reverse biased at the constant potential V_R =3.2 V.

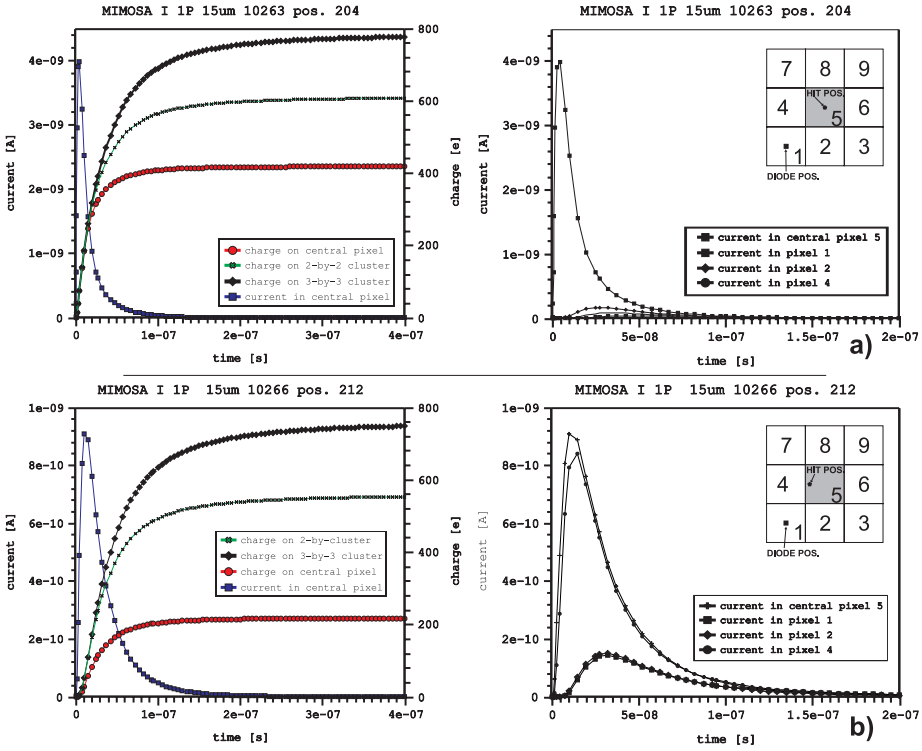

Figure 4-6: Transient simulation results for the single-diode pixel configuration with a 15 μm epitaxial layer thick. Collected charge and selected contact currents for the (a) central and (b) the side particle impact.

The currents and collected charge are presented for the central pixel only, the sum of the four pixels exhibiting the highest signals, and the sum of all nine pixels closest to the impact position. These cases of cluster reconstruction were also applied in the later analysis of data taken experimentally for a high-energy particle beam and X-ray photons. Two particle impact positions, which represent in some extent the most and least favourable charge collecting conditions on the central pixel, are shown for both pixel configurations. In the case of the pixel design with a single-diode, the current pulse lasts for more than 100 ns and the total collected charge on the 3 × 3 pixels cluster is slightly below 800 e^-. The charge collected on the 2 × 2 pixels cluster constitutes only about 75% of the charge collected on the 3 × 3 pixels cluster. In the case of the four-diode pixel design, the current pulses are much shorter and the total charge collected on the 3 × 3 pixels cluster is close to 900 e^-. For a given pixel size, the amount of collected charge starts to saturate at a time approximately three times shorter than in the case of a single diode, and the total charge collected on 2 × 2 pixels is

close to 90% of the one on the 3 × 3 pixels cluster.

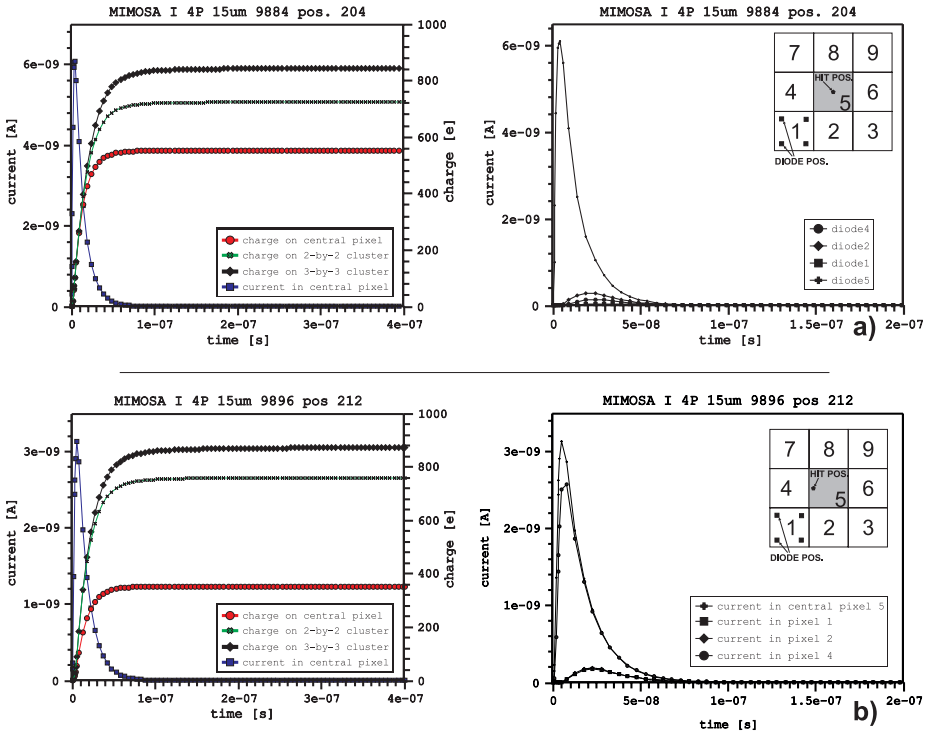

Figure 4-7: Transient simulation results for the four-diode pixel configuration with 15 μm epitaxial layer thick. Collected charge and selected contact currents for (a) the central and (b) the side particle impact.

The four-diode pixel configuration is characterised by much faster and more efficient charge collection with respect to the single diode design. However, better charge collection performance is achieved in expense of the higher total capacitance of the collecting node. In practice, this results in a deteriorated SNR for the same amount of collected charge.

Figure 4-8 and Figure 4-9 show a summary of results obtained on charge collection efficiency and the collection time for two pixel designs featuring one and four diodes. The charge collection properties were as previously analysed for three different configurations of cluster multiplicities i.e. for the single central pixel, and for 2 × 2 and 3 × 3 pixel clusters. The amount of collected charge and the collection time are plotted against the distance between the particle impact position, which was restricted to the area of the central pixel, and the middle point within the central pixel. The collection time was defined as the time after which 90% of the total charge is collected. However, the precise definition of the latter quantity is problematical due to the particular approach used to calculate charge transportation in

DESSIS-ISE. The simulator does not allow tracing single electrons resulting from the ionisation process as charge quanta. It deals with concentrations of carriers, which makes it difficult to define the time stamp when the collection process stops. The end of this process can occur either by recombination of the last carrier or by its collection on the diodes. The alternative approach, making use of the independent tracing of each charge carrier is a basis of the simulators exploiting Monte-Carlo methods [83]. Although, the electrode currents due to ionisation vanish in time, the curves depicting collected charge saturate after relatively long time from the beginning of simulation. In the present case, the amount of charge collected within 400 ns after the impact was used to define the total charge quantity. The results include numbers of collected electrons and collection time for three values of the epitaxial layer thickness. Both figures show that the charge spread among neighbouring pixels increases with the epitaxial layer thickness regardless the diode arrangement within a pixel. For a thickness of 5 μm, nearly all the collected charge is located within a cluster of 2×2 pixels. The charge collected on the central pixel depends strongly on the hit position. It is minimal for each thickness of the epitaxial layer for a corner hit, when the impact position is at equal distance from the four closest pixel centres. The charge collected in this situation is less than a quarter of the total charge found in a cluster of 3×3 pixels in the case of a single diode configuration. The situation is slightly better in the case of the four-diode configuration, where the corner hit yields approximately in 40% of the total charge found in a cluster of 3×3 pixels. The charge collected on the central pixel first increases with increasing thickness of the epitaxial layer. However, this growth is weaker for the central pixel than for clusters of 2×2 or 3×3 pixels. For a very thin epitaxial layer the total amount of collected charge in a 3×3 pixels cluster for either a single or four-diode configuration are very similar. There is almost not charge spreading outside a 2×2 pixels cluster in the case of four-diode pixel configuration. For thicker epitaxial layers, there is some improvement observed in the charge collection efficiency in favour of the four-diode configuration. In the case of the 15-μm thickness of the epitaxial layer, the total charge found on the 3×3 pixels cluster is approximately 20% higher for the four-diode configuration than to its single diode counterpart. This results from the fact that electrons are much more probably to be collected by one of the diodes in the configuration where the surface coverage by diodes is higher. The electrons are prevented from diffusing over large distances in the case of the four-diode pixel

configuration. In addition to the better charge confinement the collection is much faster in this case.

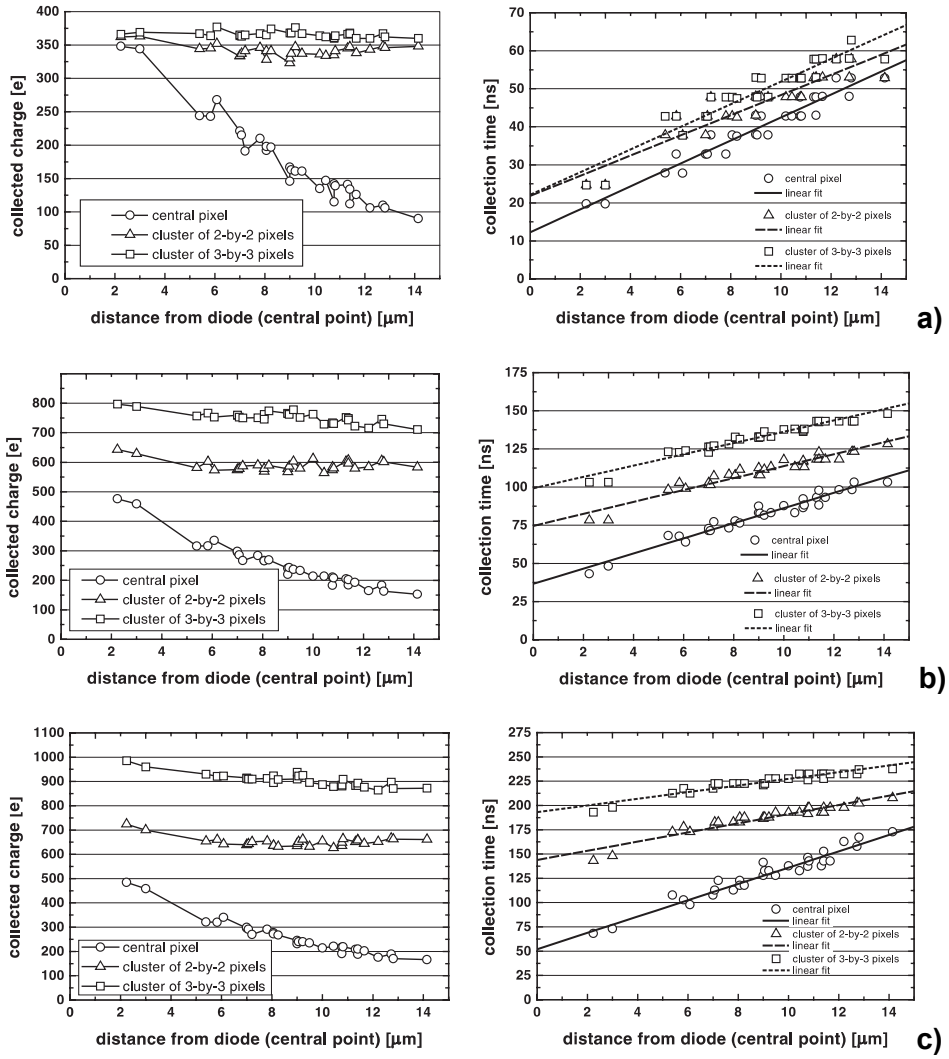

Figure 4-8: Simulated charge collection properties of single-diode pixel configuration (expressed as the number of collected electrons) and collection time as a function of the distance between the impact position and the centre of the pixel for (a) 5 μm, (b) 15 μm and (c) 25 μm thick epitaxial layers.

The collection time, increases with the epitaxial layer thickness and depends also on the impact position. In the case of the single diode configuration, the shortest collection time is observed for the central hit, i.e. when the impinging particle passes through the collecting diode. In this case, nearly all the available charge is collected on the central pixel. The longest collection time occurs for corner hits. The mean value of the collection time is less than

50 ns, 130 ns and about 225 ns for 5 μm, 15 μm and 25 μm epitaxial layer thicknesses, respectively. The charge collection time exhibits a nearly linear dependence on the hit distance from the middle point of the central pixel. On the other hand, apart from being nearly three times shorter, the collection time of the four-diode pixel configuration depends barely on a particle impact position. The nearly linear dependence of the charge collection time on the distance form the central point of the hit pixels represents a macroscopic effect, which results from superposition of charge portions collected from different depths of the simulated structure.

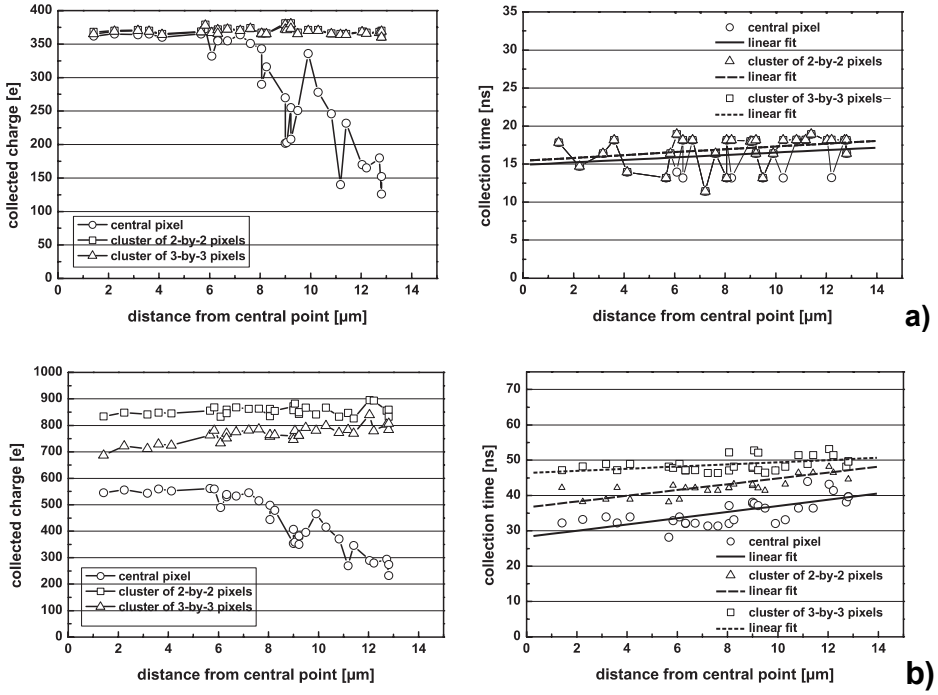

Figure 4-9: Simulated charge collection properties of four-diode pixel configuration (expressed as the number of collected electrons) and collection time as a function of the distance between the impact position and the centre of the pixel for (a) 5 μm, (b) 15 μm thick epitaxial layers.

Figure 4-10 shows simulation results obtained for the single diode pixel configuration only with the substrate thickness reduced close to zero. Plots presented in this figure allow to estimate charge collection properties for electrons originating in the epitaxial layer only. In this way, the relative contribution of the highly doped substrate to the total charge collected can be evaluated. It turns out, that despite of the very short electron lifetimes in the highly doped substrate, some carriers are able to migrate into the epitaxial layer. As a result, the

small potential well in the epitaxial layer traps those electrons, and they diffuse towards the n-well/p-epi diodes. The relative substrate contribution increases with decreasing thickness of the epitaxial layer. For a 5-μm thick epitaxial layer, the substrate contribution is estimated at the level of 30% of the total charge in the 3×3 pixels cluster. It decreases for thicker epitaxial layer, reaching 15% and 10% for 15 μm and 25 μm thicknesses, respectively. The substrate contribution becomes more important for deep sub-micrometer CMOS fabrication processes, where the epitaxial layer thickness is strongly reduced.

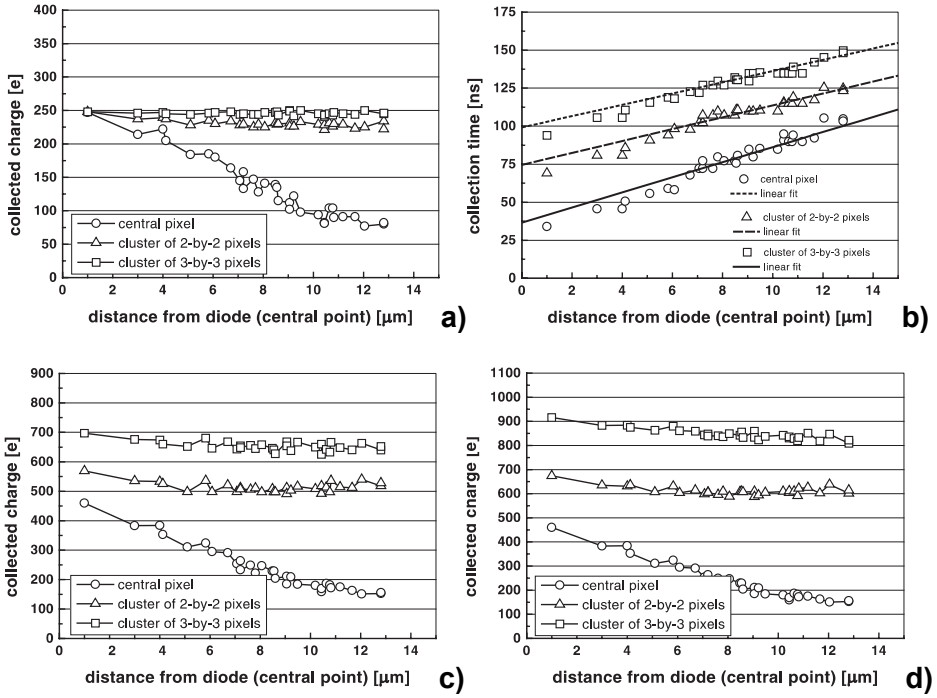

Figure 4-10: Simulated charge collection properties of single-diode pixel configuration (expressed as the number of collected electrons) for (a) 5 μm thick epitaxial layer, collection time for (b) 5 μm thick epitaxial layer and charge collection for (c) 15 μm and (d) 25 μm thick epitaxial layers with the thickness of the highly doped substrate reduced to zero.

In order to estimate more precisely the contribution of carriers originating in the substrate and the charge spreading properties, a set of simulations was carried out for the single diode pixel configuration with the substrate and epitaxial layers thickness as parameters. Only one selected impact position for the particle passing in the middle of the central pixel was considered. The results shown in the upper plot in Figure 4-11 were obtained for a fixed thickness of the epitaxial layer of 5 μm. The thickness of the substrate used in the simulation was varied. The values of the collected charge for different cluster

multiplicities are almost identical. In the case of an epitaxial layer of 5 μm thickness, the charge from the substrate constitutes about 1/3 of the signal on the central pixel. According to the simulations, only about 5 μm of the highly doped substrate gives a significant contribution to the collected charge. This effect is consistent with the low value of the electron lifetime resulting in the recombination limiting the charge spread in this layer. The distance of 5 μm corresponds to two or three diffusion lengths in the substrate and is much shorter than the usually used pixel pitch. Important information presented in the bottom part of Figure 4-11 is the amount of collected charge on the central pixel as a function of the epitaxial layer thickness. The collected charge increases with increasing thickness of the epitaxial layer. However, already for about 15 μm of the epitaxial layer the signal saturates at the level about 650 e^- and the collection time is below 150 ns. For the thicker epitaxial layer, the signal and the collection time are much higher on the 3 × 3 pixels cluster than on the central pixel. Only little saturation is observed for this cluster size even for the epitaxial layer thicker than 20 μm.

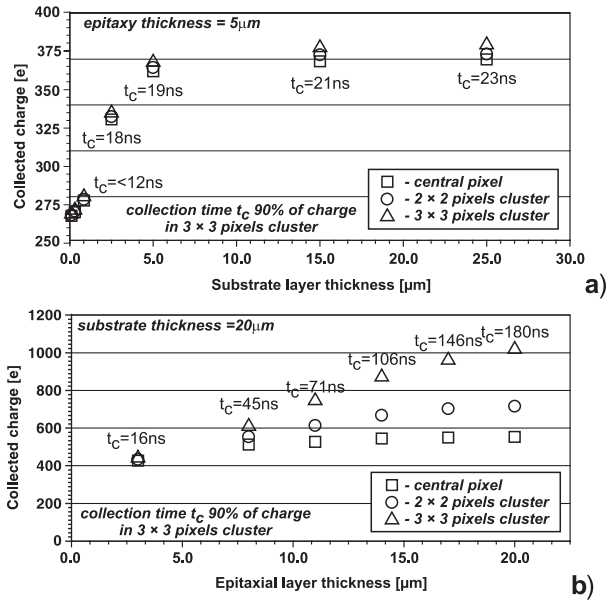

Figure 4-11: (a) Substrate contribution to the cluster charge and (b) cluster charge as a function of the epitaxial layer thickness for single-diode pixel configuration and central, passing through the diode particle track.

4.2.4 Summary of Charge Collection Simulation

The simulations have allowed to study the behaviour of MAPS detectors for efficient charged particle detection. Although the charge collection is mainly due to carrier diffusion and random walk at thermal velocity, the simulations show that the collection time can be less then 150 ns and the total charge close to 1000 electrons in a cluster of 3×3 pixels for a pixel pitch of 20 μm and the epitaxial layer thickness of 15 μm. For correctly selected detector geometry, the charge spreading is limited to a few pixels only. This property is important for guaranteeing a good multi-track resolution within dense particle jets. The pixel collecting most of the charge is usually identified as the seed pixel by a cluster reconstruction algorithm in the analysis of the experimental data. Depending on the actual detector design, the central pixel collects between 25% and 70% of the total 3×3 pixels cluster charge. The charge spreading on the neighbouring pixels can be reduced further using an optimised configuration with more than one diode in each pixel. The side effect is an increased capacitance of the collecting node resulting in a decreased voltage signal, thereby decreasing SNR.

The fabricated MAPS prototypes were exposed to a high-energy particle beam. Some discrepancies in absolute values between the experimental results presented in Chapter 6 and the results of the simulation are mainly due to the limited precision of the physical model and incomplete data on material properties used in the simulation. The data on trap levels and recombination centre densities in the silicon were not available to be included into the simulations. It seems that the essential contribution to the observed small disagreements comes from imprecisely modelled transition zones, e.g. between the substrate and the epitaxial layer. Because of lack of any data on the form of this zone, the simply abrupt junction was used in the simulation program. While in the real device, this transition zone is actually smooth, because of the dopants diffusing from the substrate during the process of the epitaxial layer growth. This process is conveyed in increased temperature making diffusion more effective. The measured doping profiles on the fabricated chip show differences between those used in the simulation. All these parameters influence somewhat the charge collection efficiency, however the results presented in this chapter still give a good approximation of the measured values, allowing optimisation to the detector design.

Chapter 5

ARCHITECTURES AND PARAMETERS OF FABRICATED MAPS PROTOTYPES

5.1 Introduction

Active Pixel Sensors were proposed at the beginnings of 90's as viable competitors for widely used CCDs in digital still photography and video applications. In that time their parameters in terms of image quality and noise were far behind those that were offered by CCDs. However, the advancement of vision chips in industrial applications, and the resourceful circuit and device libraries of CMOS processes are pushing APS to provide now cheap and powerful solution for imaging systems [84, 85].

In standard CMOS processes, several device configurations can be used as photosensitive elements; three of them being the most commonly used are shown in Figure 5-1. The first structure is a photogate (PG), which operation principle has in fact been borrowed from CCD processes. A photogate is a MOS capacitor exposed to the light[*]. The photo-generated charges are stored in a potential well, which is produced by applying a sufficiently large positive voltage to the gate of the device. The accumulated charge is transferred through the TX transistor to the readout node by applying an appropriate sequence of voltages on the PG and TX electrodes. The read-out node needs to be emptied from charges by a sequential reset operation, which defines the potential distribution during charge accumulation and read-out, as sketched in Figure 5-1a. Absorption length of a visible light in silicon depends on the wavelength and varies from a fraction of micrometer for deep blue light to several micrometers for red light. For visible light applications, sufficiently high signal response is already provided by shallow p^+/n-well or n^+/p-well diodes as shown in Figure 5-1b. The

[*] For choosing fabrication process to design a photogate device, special attention must be paid to the doping profile below the gate. Only those processes which allow access from the surface to the lightly doped substrate are useful. The access is usually realised by blocking creation of any well under the gate area. Otherwise, the depletion zone attracting charges would be very shallow or voltages to apply would be high due to increased doping level. Particular problems may be encountered for retrograded wells placed below the gate, where the doping level in the well increases with distance from the surface. When the gate is biased for read-out, the minimum potential is settled inside the bulk. This makes charge flow through the transfer transistor ineffective. Additionally, for particle tracking application demanding 100% fill factor, only a photogate device collecting charge from the whole volume underneath the pixel can be used, thus possibility of the blocking well creation is essential in that case.

thickness of an active volume limited to the depletion zone of p-n junctions is small, but the diodes occupy a significant fraction of the total pixel area, which is usually between 30% and 50%. This solution is very flexible as regards to the possibility of integrating some signal processing functionalities built into each pixel. The designer can take advantage of both transistor types available to implement signal processing functions, but the ratio between the area sensitive to light and occupied by the read-out electronics must be balanced. The fill factor in the case of a photodiode shown in Figure 5-1b is determined by the area occupied by the read-out electronics, and thus it is usually in the order of a few tens percent. Additionally the quantum efficiency* of this configuration is limited by the small thickness of the active volume, which has a negative impact especially for the red light detection.

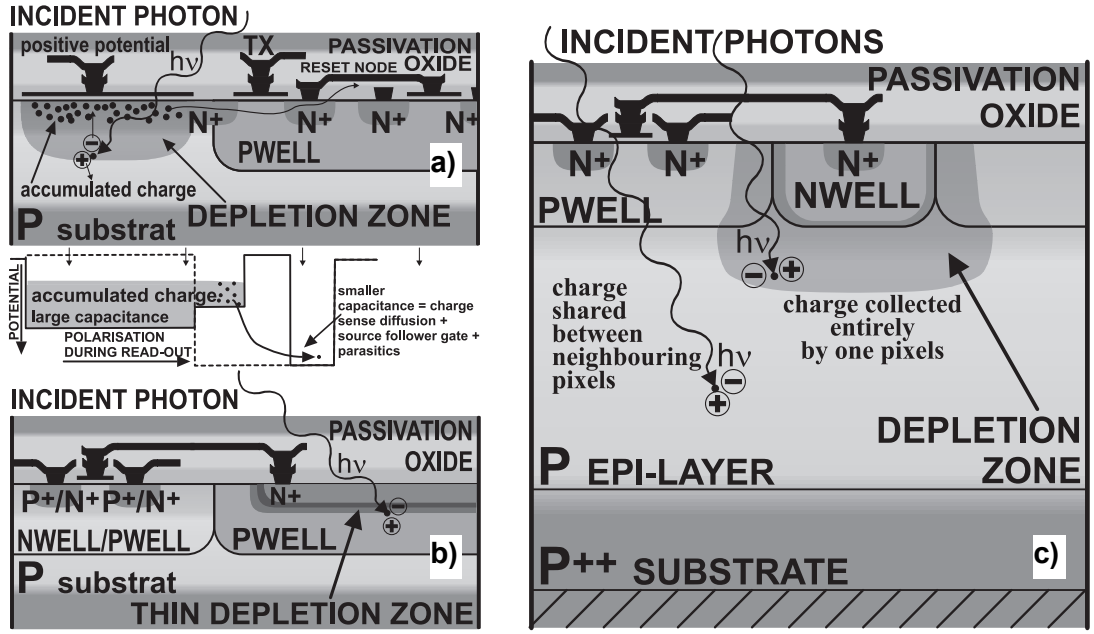

Figure 5-1: Principle of visible light photons detection achieved applying (a) photogate (PG) element, (b) n^+/p-well photodiode and (c) n-well/p-epi photodiode for charge collection.

A solution allowing 100% fill factor [72] for the visible light detection is shown in Figure 5-1c. The idea is fully compatible with all standard CMOS fabrication processes featuring twin complementary tubs on an epitaxial layer or on a high resistivity substrate†. The limiting

* Quantum efficiency is defined as the ratio [%] between the number of generated charge carriers (usually electrons) and the number of impinging photons.

† High resistivity substrate for CMOS process, in contrast to fully depleted detectors, addresses a doping level in the order of $10^{14} – 10^{15}$ cm^{-3}.

factor of this approach is the restriction to the use of only one type of transistors i.e. NMOS transistors in the pixel. This makes it difficult to implement an advanced signal processing blocks close to the place where the charge is sensed.

The efficiency of using the scheme of Figure 5-1c for charged particle detection was verified in physics simulation, as described in Chapter 4. Following the promising simulation results, the n-well/p-epi diode was chosen as a key element for designing and fabrication of a series of the prototype MIMOSA chips. The development has been oriented towards applications in high-energy physics and other imaging purposes in physics and medical domains. The design work included evaluation of the device characteristics, which was carried out in theoretical calculations, electric network simulations (SPICE-type) and additional physics simulations (ISE-TCAD). These analyses were focused on the estimation of the charge-to-voltage conversion gain, finally achieved by two crosschecking methods, on the optimisation of SNR and read-out speed and on prospecting for optimal read-out architecture.

5.2 The MIMOSA Chips

5.2.1 General Design Aspects

Following the idea of an n-well/p-epi diode as the charge collecting element, four prototype chips, called in turn MIMOSA I, II, III and IV, were designed and fabricated. A different CMOS process was used for fabrication of each chip. Chronologically, the first device was implemented in a process with the feature size of 0.6 μm and then processes 0.35 μm 0.25 μm and another 0.35 μm were used in succession. All chips were arranged in a form containing several independent arrays of pixels having slightly different designs. In the case of MIMOSA I and IV the chips feature four separate matrices, and correspondingly, there are six and two matrices for MIMOSA II and III, respectively. The number of active elements in each array is 64 × 64 with a pitch of 20 μm in the case of MIMOSA I, II, and IV, and 128 × 128 pixels laid out with a pitch of 8 μm in MIMOSA III*. In either case, the pitch

* In MIMOSA III and IV the first column pixels were left floating and the read-out line is tied to the fixed voltage, when any of the first column pixels is selected. This yields in the vertical pattern in acquired images allowing an easy recognition and correction of potential problems with chip synchronisation during the tests. Therefore, the useful signal is sensed only by 128 × 127 pixels and 64 × 63 in the case of MIMOSA III and IV, respectively.

was chosen uniform in both directions. The moderate number of active elements in each array was chosen opting for chip simplicity, reduced fabrication costs and extensive testing options of the first prototypes. On the other hand, the area covered by arrays of active pixels could not be too small bearing in mind statistical tests and measurements performed with radioactive sources and high-energy particle beams. The pixels were supposed to cover at least a few square millimetres, in order to carry out tests with a high-energy particle beam in an efficient way. For these tests the surface of the examined detector should be compatible with the size of the plastic scintillator delivering the coincidence signal. More details on the test set-up configurations are provided in Chapter 6.2. The higher number of pixels in the active array facilities also tests with radioactive sources, because it provides higher hit statistics and it allows performing some basic imaging tasks. It is also important to perform statistical studies with higher pixel population including the pixel-to-pixel gain and DC level variations. The detailed block diagrams of all fabricated chips, including chip pin-outs and layouts of single pixel cells are given in Appendix-C.

The most important design features of fabricated chips are summarised in Table 5-10. Each individual pixel is comprised of only three MOS transistors and a floating diffusion n-well/p-epi diode. The detailed description of the chips design, particularly of MIMOSA I and III, can also be found in [86] and [87], respectively. As mentioned before, because n-well implantation areas are used for the collecting diodes, the design is limited to NMOS transistors only at the pixel level, whereas both types of transistors are used on the chip periphery. The goal of the first two prototypes was to demonstrate experimentally the feasibility of the new technique for charged particle detection. The design of the two other prototypes was more oriented to test some features, whose implementation resulted from experience gathered in the first stage of work. This included the possible use of deep sub-micron processes with only thin epitaxial layers for MAPS manufacturing, design improvements oriented towards the increase of radiation hardness and noise performance, and tests of alternative charge sensing elements. All chips feature additional specific test structures placed at the device periphery. Test structures include some pieces of the whole chip design, like output amplifiers, arrays of transistors and some critical parts of pixels, as well as several large arrays of a few thousands of diodes and transistors connected in parallel. These large arrays were prepared in MIMOSA III for studying irradiation effects, mainly for

measurements of the radiation induced leakage currents. The diodes in the test structures have the same size and the diode arrays are laid out with the same pitch as it was used for the detecting matrices. Thus, the diode test structures resemble as closely as possible arrays of active detector elements, they only lack of all read-out transistors. The space between diodes was filled with p^+-type implantation to form a guard-ring biased to the ground, and as an option some diodes were encircled by a polysilicon ring. The latter introduces thin oxide area in the closest vicinity of the diode. Implementation of these design features was motivated by striving for identification of leakage current paths within the pixel for irradiated detectors.

Table 5-10: Design features of the fabricated MIMOSA prototypes.

Chip features	MIMOSA I	MIMOSA II	MIMOSA III	MIMOSA IV
Fabrication process	AMS 0.6 µm CUP, 3M+2P, 5V	AME 0.35 µm AD, 5M+2P, 3.3 V	IBM 0.25 µm CMOS 6SF, 3M+1P+MQ, 2.5 V	AMS 0.35 µm CSX, 3M+2P, 3.3 V
Epitaxial layer	14.0±2.0 µm (~7.6 ×10^{14} cm^{-3})	4.0±0.2 µm (~10^{15} cm^{-3})	2.0±0.2 µm (~10^{15} cm^{-3})	no epitaxial (~10^{14} cm^{-3})
Chip configuration	4× 64 × 64 pixels, pitch 20 × 20 $µm^2$, square layout	6× 64 × 64 pixels, pitch 20 × 20 $µm^2$, square and staggered layouts	2× 128 × 128 pixels, pitch 8.0 × 8.0 $µm^2$, staggered layout	4× 64 × 64 pixels, pitch 20 × 20 $µm^2$, square layout
Sensitive element	3.1 × 3.1 $µm^2$ n-well/p-epi diode	1.7 × 1.7 $µm^2$ n-well/p-epi diode	1.0 × 1.0 $µm^2$ n-well/p-epi diode	2.0 × 2.0 $µm^2$ n-well/p-sub diode
Die size	3.6 × 4.2 $µm^2$	3.5 × 4.9 $µm^2$	4.0 × 2.0 $µm^2$	3.7 × 3.8 $µm^2$
Radiation tolerant design	no	yes (analogue part)	yes (full)	yes (full)
Implemented structures	1 and 4 diodes / pixel	• 1 and 2 diodes / pixel • structures for irradiation tests (parallel diodes) • current mode pixel (photoFET)	• 1 diode / pixel • structures for irradiation tests (parallel diodes) • varied size of source follower transistor	• 1 and 3 diodes / pixel • charge spill gate • current mode pixel (photoFET) • auto-reverse-polarised diodes
Read-out and clocking speed	Serial analogue read-out f_{clk} < 5 MHz	Serial analogue read-out f_{clk} < 25 MHz	Serial analogue read-out f_{clk} < 40 MHz	Serial analogue read-out f_{clk} < 40 MHz
Gain of output amplifier	× 4	× 4	× 5	× 5

5.2.2 Read-out Architecture

All MIMOSA chips are equipped with a serial analogue read-out, requiring, apart of a few lines used to bias the circuitry, only two digital signals to operate. The clock (*CLOCK*) signal is used for addressing consecutively pixels for read-out and for selecting rows to restore the reverse bias on the charge-sensing node during the reset phase. While, the reset

phase is initiated by pulsing the reset (*RESET*) signal. The way in which each MIMOSA chip responds to the *RESET* signal is slightly different. Although, for the external driving circuitry, the differences are only limited to the number of necessary empty clock cycles after applying *RESET* and before the internal reset phase is started. Generally, the reset signal should be held high at least for two clock cycles to start properly the reset phase. Then each row of pixels is reset during a time equal to the duration of the reset pulse, i.e. at least for two clock cycles in the case of MIMOSA III and IV and exactly for one and two clock cycles in the case of MIMOSA I and II, respectively. Each MIMOSA chip is equipped with the output of two internal signals called *LINE_SYNCHRO* and *CHIP_SYNCHRO*, which are activated when the first addressed row and the first addressed pixel are selected for read-out, respectively. The additional *SHUTTER* signal, available in MIMOSA III, is used to activate the operation mode with an electronic shutter, in which the entire row of pixels can be reset immediately following its read-out. Such a simple read-out arrangement used in four small-scale detector chips, allowed easy operation of the devices and was sufficient for demonstrating feasibility of the new detection technique*.

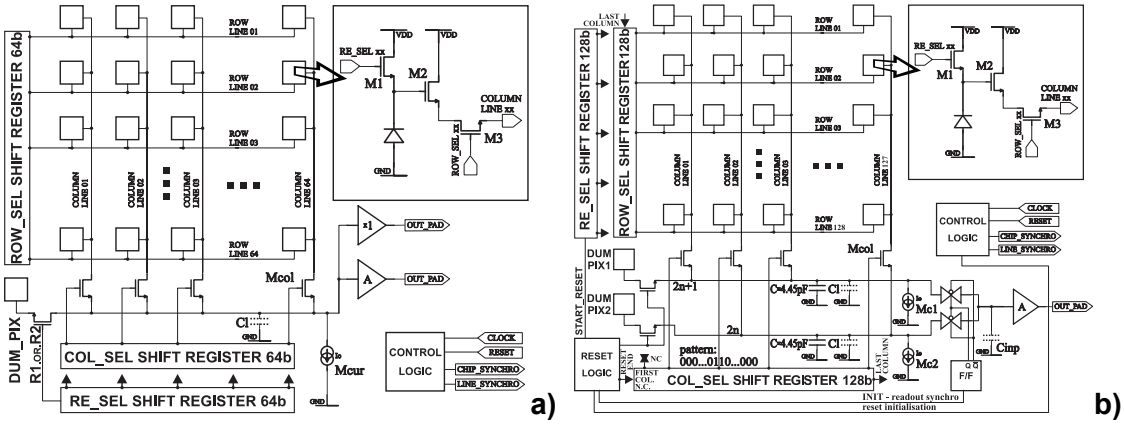

Figure 5-2: Schematic diagrams of (a) MIMOSA I and (b) MIMOSA III.

Analogue power supplies, bias signals and analogue outputs were carefully separated in each chip. The appropriate lines were routed independently for each array, which was dictated by the requirement to assure correct operation of the remaining arrays in case of a malfunctioning of one. Although, the digital parts used for control and addressing are also

* It is worth noting that in future designs the readout will be optimised to satisfy specific requirements related to each application. For example, adding parallel column-wise data handling or including some data processing directly on a chip.

independent for each pixel array, they are powered from common digital power supplies and driven from common control lines, i.e. *CLOCK* and *RESET* lines. The schematic diagrams of MIMOSA I and MIMOSA III are presented in Figure 5-2. The differences in conceptions of both chips showed in this figure are only slight. The list of them includes modifications in internal control logic blocks with some set-up lines added, rearrangement of the reset operation from column-wise to row-wise order, which is in accordance with row addressing of pixels for read-out, and the use of the second read-out line switched alternatively through the output amplifier to the analogue output pad of the chip. The schematic diagram of the MIMOSA III chip can be used after small modifications, consisting in adjustment of number of pixels in an array, the use of a dummy pixel, etc., to represent the internal configuration of MIMOSA II and IV as well.

The floating diffusion of the collecting diode has to be reset periodically to remove the collected charge and to compensate the diode leakage current. This procedure superimposes thermodynamic fluctuations onto the signal described statistically by [88]

$$\overline{V_n^2} = \frac{kT}{C_d}, \tag{5-1}$$

where C_d is a node capacitance and V_n represents the noise voltage. This type of noise dominates in the pixel the contributions from other sources and is known as the kTC noise. Fortunately, it can be effectively removed applying Correlated Double Sampling signal processing (CDS) [89, 90]. For all MIMOSA circuits, the CDS operation has to be performed by software during off-line data processing, and the useful signal is calculated as the difference between two consecutive frames taken after the reset. The detector operated in this mode is a linear charge-integrating device with an integration time equal to the readout time of one full frame, determined by

$$\tau_{int} = \frac{N_{pix}}{f_{clk}}, \tag{5-2}$$

where N_{pix} is the total number of pixels connected to one serial output line and f_{clk} is the read-out clock frequency.

5.2.3 Read-out Timing Sequence

In the case of MIMOSA I, II and IV, two 64, and in the case of MIMOSA III, two 128

bit long shift registers, selecting rows and columns, are used for pixel addressing and one shift register is used for selecting rows for reset. In the case of MIMOSA I and II, the whole array is reset in 64 clock cycles, when the reset shift register selects the entire row at a time. For MIMOSA III and IV, the acceptable duration of the reset pulse can be longer than the default two clock cycles. In this case, each pixel is reset for the time corresponding to the actual length of the reset pulse and as a consequence, the entire reset phase becomes accordingly longer. The analogue information is read out in successive clock cycles, where consecutively addressed pixels are multiplexed onto the common output line. In the MIMOSA I chip design, a very simple read-out scheme was used, where a pixel selected for readout is connected directly to the read-out line and the output amplifier. The parasitic capacitance load of read-out lines depends on the dimensions of the chip and usually represents values in the order of a few picofarads. Switching between consecutive pixels requires adapting of the read-out line potential to the level imposed by the source follower transistor currently driving the line. Due to the limited strength of source followers and relatively high dispersion of their output voltages, the maximum read-out speed for this read-out scheme is limited, in practical cases, to about 10 MHz only. The sequential addressing of pixels for read-out, allows obtaining charge integration time equal to the time needed for one full read-out cycle of all pixels in the array, i.e. frame read-out time.

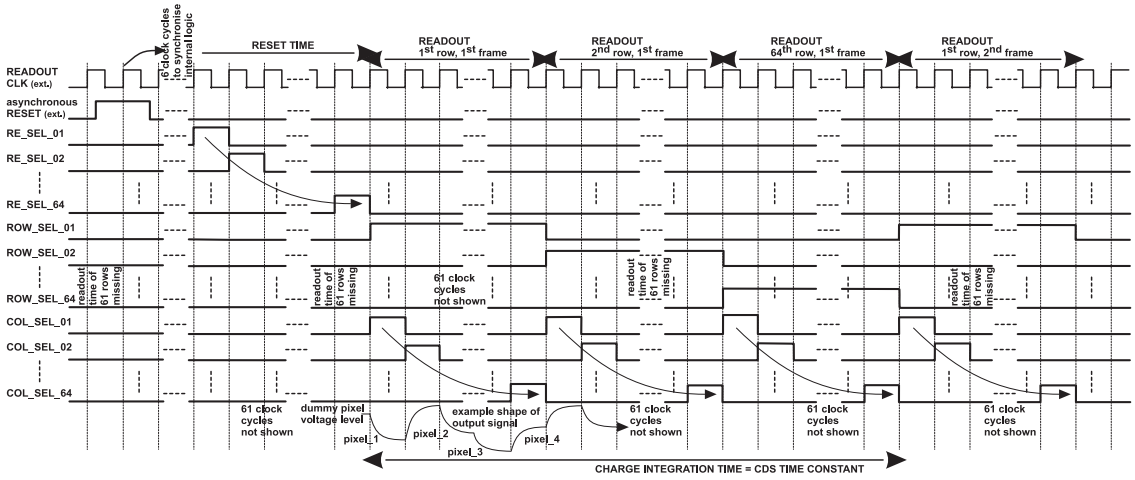

Figure 5-3: Timing diagram for MIMOSA I resulting in charge integration time equal to one full frame read-out time.

The example timing diagram for the MIMOSA I chip, which results in charge integration time equal to one full frame read-out time, is shown in Figure 5-3.

Starting with the MIMOSA II chip design, two separate read-out lines were introduced, that are switched alternatively to the output amplifier by means of two transmission gates. This approach results in the read-out architectures of MIMOSA II, III and IV such, that all odd columns are connected to the first line and all even columns are linked to the second one. This solution has been introduced to allow to overcome limitation of the read-out speed and to improve the noise performance by the possibility of the additional capacitive charge of the read-out lines. The sequential addressing of pixels for read-out is preserved, but each pixel is connected to the appropriate read-out line for the time of two clock cycles. When a chosen column is being read out, the following one is being prepared by switching on the bias current passing through the pixel source follower transistor, which allows to charge the capacitive load of the line to the level corresponding to the voltage of the source follower in the addressed pixel. The two read-out lines in Figure 5-2 are switched alternatively to the output amplifier. The output amplifier represents only small input capacitance allowing fast signal settling. Two transfer gates driven from a synchronised with the read-out clock flip/flop are used fro selecting appropriate read-out line to be connected to the output amplifier. This approach results in an increased read-out clock frequency of a few tens of MHz. While, the number of clock cycles required to perform one full frame read-out remains not changed. The timing diagram proposed for the MIMOSA III chip is shown in Figure 5-4.

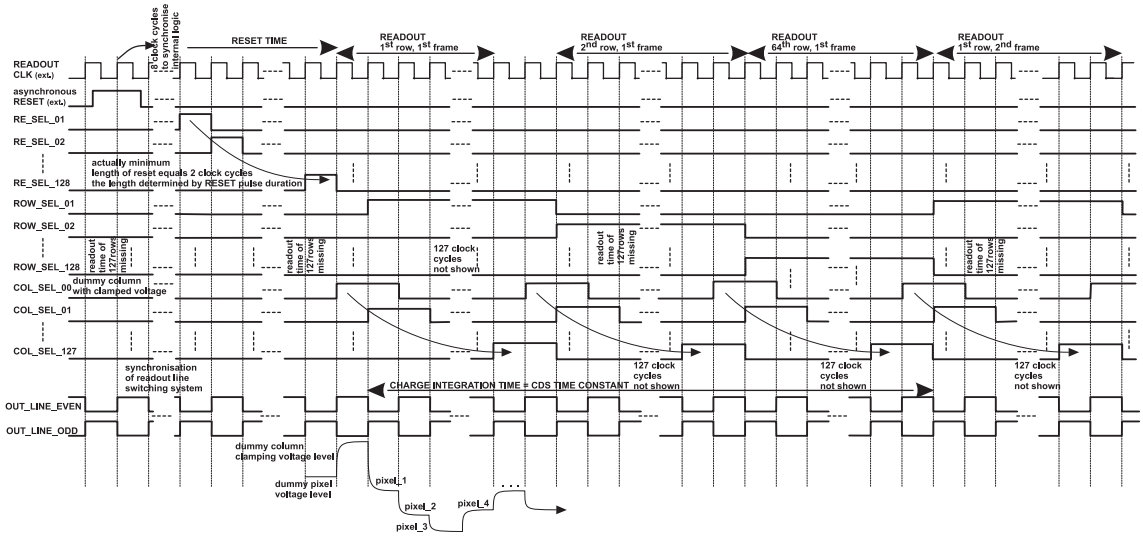

Figure 5-4: Timing diagram for MIMOSA III exploiting alternate read-out scheme.

The preparation phase for reading out a single pixel amounts to two clock cycles in the case of MIMOSA II, III and IV. However, in the case of much higher capacitive load it can be extended, as is proposed for the design of the MIMOSA V chip presented in Chapter 7.2.

Additional capacitances in Figure 5-2 are used to increase the capacitive load of both read-out lines, so that to limit the bandwidth of the source follower. The load capacitances result from the noise optimisation procedure presented in Chapter 5.4, and the actual values vary for each chip. In the case of MIMOSA III, the loading capacitance can be switched between two values, using a transmission gate, to adapt the capacitive load to the clocking speed. The chosen bias current of the on-pixel source follower results from a trade-off between the noise performance, the maximum read-out speed and the required signal swing for which a correct polarisation in saturation is maintained for all transistors. On one hand, the increased bias current decreases the noise spectral density of the source follower; on the other hand, the reduced bias current in combination with the column line parasitic capacitance decreases the cut-off frequency of the source follower and increases its signal swing. The bandwidth of the source follower was restricted to the maximum extent preserving the assumed read-out speed. The analogue read-out channel was optimised for the maximum clock frequency of 5 MHz, 25 MHz and 40 MHz for MIMOSA I, II, and III and IV, respectively. In each chip, an output non-inverting buffer, built with a low noise, custom designed operational amplifier and a resistive ladder provides voltage gain of 4 for MIMOSA I and II and 5 for MIMOSA III and IV.

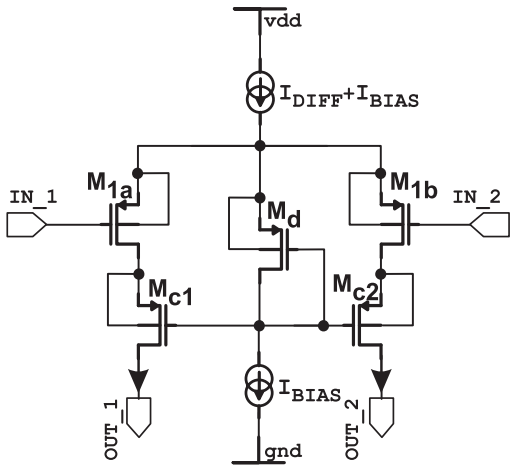

Figure 5-5: Differential cascode with common mode biasing principle.

It was optimised to drive the input capacitance of an off-chip amplifier. The input differential

stage of the operational amplifier is shown in Figure 5-5. It is a classical circuit built with a PMOS cascode exploiting dynamic polarisation of the cascode transistors M_{c1} and M_{c2}, which adapts their bias to the common mode voltage on the amplifier input through the diode transistor M_d. The input capacitance of the on chip output buffer is small, especially when compared to the read-out line load. Thus, it is charged in a short time after the transfer gate connecting the selected read-out line is activated. The multiplexing technique of two read-out lines, combined with an optimised design of the output amplifier, allowed to increase the read-out clock frequency up to 40 MHz for the latest chips, to be compared to 5 MHz only in the case of MIMOSA I.

5.2.4 Pixel Cells Design

Each chip features slightly different configurations of arrays of pixels. The MIMOSA I and IV chips were designed having only square pixel layouts, of which an example is shown in Figure 5-6a. A staggered pixel layout was introduced for the MIMOSA II chip, where it was used for two of total four arrays implemented in the chip. In the consecutive step, the arrays in the MIMOSA III chip were designed using only staggered layout. The staggered pixel layout, of which an example is shown in Figure 5-6c, was introduced searching for cluster configurations, in which the number of pixels with only partial signals due to charge sharing is reduced. This approach should result in optimum SNR and better spatial resolution. In the staggered layout, every other row is shifted by half the pixel pitch. In this way, each pixel has only six closest neighbours, reducing potentially the number of pixels in the reconstructed cluster during the data analysis. Apart of different layouts of arrays of pixels implemented in each chip, the topology of the basic cell was also varied. The basic pixel configuration for all chips features one collecting diode of the minimum achievable size in a given fabrication process per pixel, as it is shown in Figure 5-6a. The standard single-diode pixel is the only configuration implemented in MIMOSA III, but the size of the source follower transistor was varied in this chip. Five different dimensions were used to test the influence of this parameter on the pixel noise performance. The second configuration used in MIMOSA I, is a design with four charge collecting diodes placed close to each pixel corner and all connected to a common source follower gate as it is shown in Figure 5-6b. In MIMOSA II, apart of the default single diode configuration, the pixel designed with two

charge-collecting diodes was also used. Then, MIMOSA IV was designed with two variations of a basic cell, i.e. with one and three diodes per pixel. Pixel configurations with more than one charge collecting diode were introduced to test the reduction of charge collection time and to take benefit of better confinement of the charge. Normally, The spread among several neighbouring pixels is observed. The price to pay in the case of multiple diodes per pixel is increased equivalent noise charge due to the higher node capacitance worsening the charge-to-voltage conversion gain.

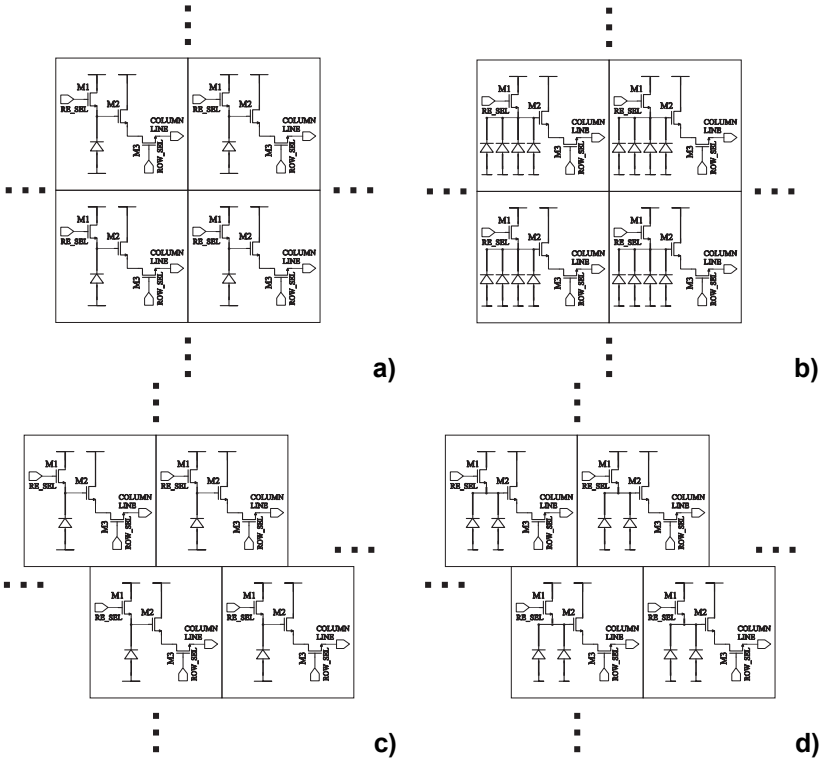

Figure 5-6: Pixel configurations and array layouts (a) and (b) square and (c) and (d) staggered in MIMOSA I (a) and (b), MIMOSA II (a), (c) and (d), MIMOSA III (c) and MIMOSA IV (a).

Although the radiation environment in experiments, for which the MAPS detectors are being developed, will not be as harsh as in the LHC experiments, the radiation hardness of the new devices was considered to be an important issue. As the first prototype, MIMOSA I was fully designed disregarding radiation tolerance constraints, and the standard layout techniques with rectangular NMOS transistors were applied. The investigation of problems related to the radiation hardness was started with the MIMOSA II chip. The remaining chips, including MIMOSA II, were prepared and contained at least some parts dedicated to study the possibility of increasing the radiation hardness of the MAPS devices. This includes the

use, for some arrays of active elements, of special layout rules requiring NMOS transistors designed in the radiation tolerant enclosed geometry and p^+-type guard-rings. In the case of MAPS tracking devices, apart of high radiation hardness of the electronics, the preservation of an efficient charge collection from the epitaxial layer underneath the electronics is of the primary importance. The use of different fabrication processes for the MIMOSA chips manufacturing, offered the opportunity to compare charge collection from the epitaxial layer for each process and its immunity to irradiations. Additionally to the loss of efficiency of charge collection from the epitaxial layer, an important increase of the leakage current of the charge collecting diode leads to shorter saturation times and an increase of the shot noise. Those are unwanted effects on the device operation. In order to investigate further the radiation effects, modified designs of the charge collecting diodes were implemented in the MIMOSA III RH chip version*. Layouts of this modified pixel configurations are described in Appendix-C. Their designs are focused on two ideas. In the first idea, a poly-silicon belt placed around the diode cuts the surface leakage current paths induced by positive charge built-up on the thick oxide after irradiation. The embodiment of the first idea is shown in Figure 5-7, where the thin oxide is is placed around the n-well/p-epi diode. The polysilicon gate is used to drive the silicon volume region beneath the thin oxide layer in accumulation.

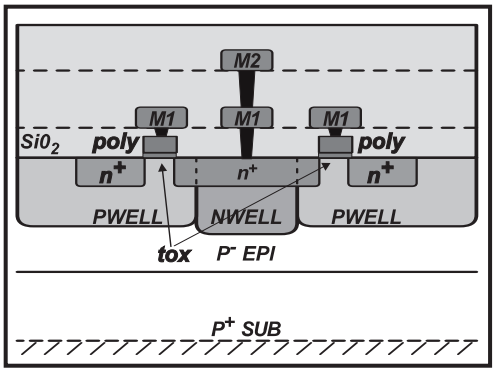

Figure 5-7: Pixel design with thin oxide in the vicinity of the charge collecting diode.

The second idea removes abrupt oxide implants of Shallow Trench Isolation (STI) from the vicinity of the diode. The removal of STI is expected to limit the charge built-up close to

* Actually the MIMOSA III chip was fabricated in two versions. The first chip version called MIMOSA III is a standard design, where the emphasis was laid on the optimisation of noise and read-out speed. The second chip MIMOSA III RH features ideas implemented to test possible improvements in radiation hardness of the basic detecting elements.

the diode and to reduce the density of interface states, which could play a role of generation-recombination (G-R) centres increasing the leakage currents. The detailed view of the latter idea is presented in Figure 5-8, where the standard diode design is compared to the one with the suspicious oxide parts removed. Practical realisation of the proposed solution from Figure 5-8b usually needs to violate several DRC rules of the process used, thus it can be applied only for some processes for which a specific mask arrangement allows such or similar configuration. The generation of the separated silicides areas over n^+-type and p^+-type diffusions, which are in direct contact, was considered as the most critical point of the design. The desired effect was achieved by introducing a special layer mask between the critical regions preventing formation of silicides in those places. The structure from Figure 5-8b leaves open the question of the electrical properties on the formed n^+ - p^+ interface.

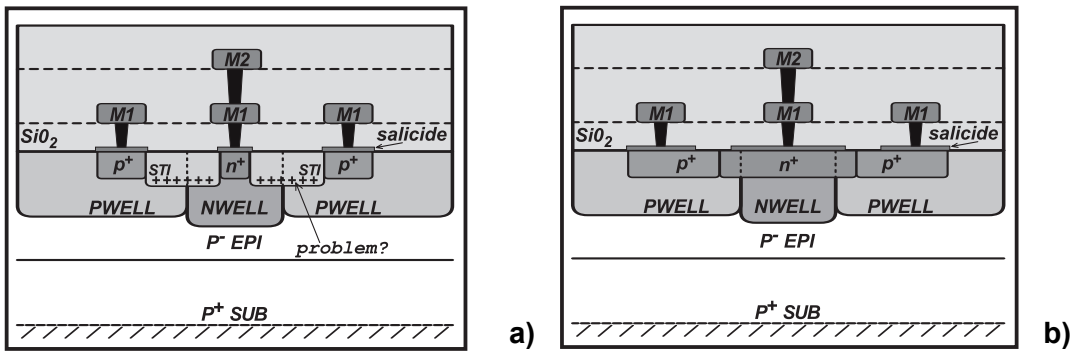

Figure 5-8: Standard configuration of the n-well/p-epi collecting diode with p^+-type guard-ring implemented in a sub-micrometer process (a) with STI and (b) modified design with extended n^+-type and adjacent p^+-type implantation areas.

5.3 Charge-to-Voltage Conversion Gain Calibration

5.3.1 Definition of the Charge-to-Voltage Conversion Gain

The collected charge, Q_{coll}, as shown in Figure 5-9, is sensed in the pixel as a voltage variation on the diode. This voltage, followed by the source of the M2 transistor, is available for read-out. The charge-to-voltage conversion gain is defined by

$$G_{q\to V} = \frac{\partial V_s}{\partial N_e}, \tag{5-3}$$

where V_s is the detector signal expressed and N_e is the number of collected charge carriers

i.e. electrons during the integration time. The charge-to-voltage conversion gain defines signal amplitude at the output of the imaging device for a single charge carrier collected in the pixel. The habitually used unit for this quantity is $\mu V/e^-$.

In MAPS devices with an amplifier in each element, pixel-to-pixel variations of the conversion gain may be introduced during the device fabrication. To fully characterise a sensor, the variation of individual pixel gains has to be determined. A large conversion gain is desirable in the presence of the read-out noise to maximise the SNR. The charge-to-voltage conversion gain is determined by the total conversion capacitance C_{conv} seen at the diode node during the pixel read-out and the slightly below unity voltage gain of the source follower. The C_{conv} capacitance contains two terms. The first one depends on the bias voltage, and is formed by the reverse-biased junction capacitors of the charge collecting diode C_d, and the source-to-bulk junction of the reset transistor $C_{sb,M1}$. The schematic diagram useful in determination of the conversion gain is shown in Figure 5-9. The value of the junction capacitance depends on the reverse bias voltage and the doping parameters of the technological process used for fabrication. Practically, the achievable range of the reverse bias voltages is limited by the maximum rating conditions specified for a given process. The capacitance of a junction is an inverse exponential function of the bias voltage*.

The junction capacitances, in CMOS devices, are habitually modelled in a very simple manner. The depletion region is taken to be a dielectric between two capacitor plates. The model is implemented in two parts. The first part in a model defines an area capacitance. The second component identifies a perimeter capacitance since the diodes have a form of relatively deep implants with important contribution of the sidewall junctions. Thus, the total junction capacitance in practical applications is found from

$$C_d = W\,L\frac{C_j}{\left(1+\frac{V_R}{V_{bi}}\right)^{MJ}} + 2\left(W+L\right)\frac{C_{jsw}}{\left(1+\frac{V_R}{V_{bi}}\right)^{MJSW}}, \tag{5-4}$$

where C_j is the junction capacitance per drawn area, C_{jsw} is the junction capacitance per unit area, M_j and M_{jsw} are the area and sidewall junction grading coefficients, respectively, and W

* The exponent coefficient, in the case of an ideal abrupt junction, equals $1/2$ and for the linearly graded doping profile across the junction, it becomes $1/3$. In a real junction it falls somewhere between the two extremes.

and L are the dimensions of the rectangular diode implantation area. The coefficient V_{bi} is the junction potential calculated from equation (4-18). The second part of the capacitance C_{conv} is made of the parasitic stray capacitance of interconnecting lines $C_{p,int}$, the gate-to-source overlap capacitance $C_{gs,M1}$ of the transistor M1, and the input capacitance of the source follower. The latter is actually equal only to the gate-to-drain capacitance $C_{gd,M2}$ of the transistor M2. This is due to the bootstrapping effect on the transistor M2 gate-to-source capacitance.

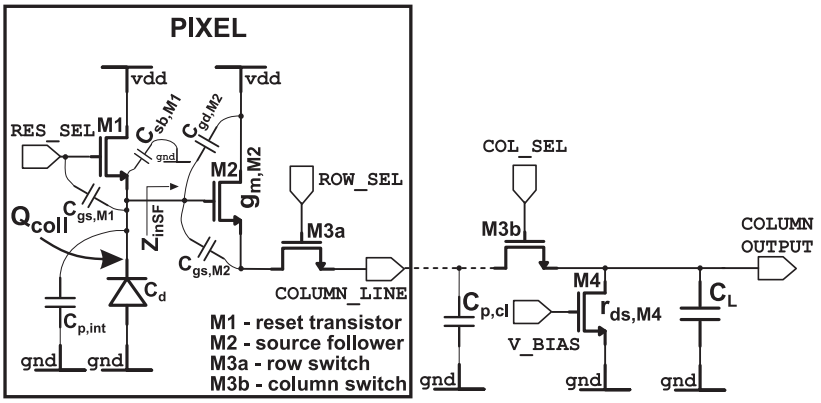

Figure 5-9: Scheme of pixel and read-out circuit with capacitances influencing conversion gain.

The latter is easily estimated in the analysis of the source follower input impedance Z_{inSF}, which in the most general case is given by

$$Z_{inSF}(s) = \frac{1 + g_{m,M2} r_{ds,M4} + s\left(C_L + C_{p,cl} + C_{gs,M2}\right) r_{ds,M4}}{s\left[C_{gs,M2} + C_{gd,M2} + C_{gd,M2} g_{m,M2} r_{ds,M4} + s\left(C_{gs,M2} C_{gd,M2} + \left(C_L + C_{p,cl}\right)\left(C_{gs,M2} + C_{gd,M2}\right)\right) r_{ds,M4}\right]}, \quad (5\text{-}5)$$

where components: $C_{gs,M2}$, $C_{gd,M2}$, C_L and $C_{p,cl}$ are the gate-to-source capacitance and the gate-to-drain capacitance of the transistor M2, the load capacitance of the source follower and the parasitic capacitance of the column line, respectively. Coefficients: $g_{m,M2}$ and $r_{ds,M4}$ are the small signal transconductance of the transistor M2, and the output dynamic resistance of the current source transistor M4, respectively. For the high values of the product $g_{m,M2} r_{ds,M4}$, equation (5-5) reduces to the simply form

$$Z_{inSF}(s) = \frac{1}{C_{gd,M2}s}. \tag{5-6}$$

The last expression shows no dependence of the pixel charge-to-voltage conversion gain on the gate-to-source capacitance of the transistor M2, and its capacitive load. An increase in conversion gain can be achieved by the minimisation of the parasitic capacitances, which are closely related to the dimensions of the active components. Unfortunately, the size of the reset and source follower transistors usually cannot be chosen to be minimal. First of all, the source follower transistor is optimised for the highest SNR. Secondly, the reset transistor is to provide an efficient and fast reset operation. Both conditions result in non-minimum polysilicon gate dimensions. Furthermore, the smallest dimensions for transistors designed with enclosed layouts according to the rules aiming for increased radiation hardness, are far from those, which are allowed by the sub-micrometer processes. Thus, to minimise the gate overlapping capacitance, the design of the source follower with the minimum drain perimeter is chosen. On the other hand, the source-to-bulk junction capacitance of the reset transistor dominates its source-to-gate overlap capacitance. Thus, the reset transistor with the minimum source area is recommended. For enclosed transistor layouts, this translates to the source of the reset transistor M1 and the drain of the source follower transistor M2 placed inside of the donut geometry of their poly-silicon gates.

The bias dependent junction capacitances give rise to a non-linearity of the charge-to-voltage conversion gain as a function of the collected charge. This non-linearity is reduced to some extent by contributions of the interconnecting lines and the poly-silicon gate overlaps in transistors, which are the linear capacitances. The junction capacitances are usually slightly smaller than half of the total conversion capacitance C_{conv}. This observation is valid under nominal bias conditions and assumption on the effective reset operation performed with a repetition rate that does not allow a complete discharge of the conversion capacitance. The estimated relation between the linear and non-linear capacitance components is shown in Table 5-11 for four MIMOSA prototypes under the typical bias conditions. The charge-to-voltage conversion gain $G_{q\to V,SF}$ referred to the output of the source follower is given by

$$G_{q\to V,SF} = \frac{g_{m,M2}}{g_{m,M2} + g_{mb,M2}} \frac{1}{qC_{conv}}, \tag{5-7}$$

with

$$C_{conv} = C_{p,int} + C_d + C_{bs,M1} + C_{gs,M1} + C_{gd,M2}, \quad (5\text{-}8)$$

where the component $C_{p,int}$ is the parasitic capacitance of interconnections within a pixel. A precise calibration of the conversion gain is one of the main issues regarding the correct characterisation of MAPS devices. The measure of the conversion gain is needed for further parameterisation of the device performance. Particularly, the calibration of the conversion gain allows to refer the measured signals due to particles detected in absolute units of numbers of collected charge carriers and to measure the leakage current of the charge collecting diodes.

Table 5-11: In-pixel capacitances - constituents of C_{conv}, for fabricated prototypes at typical bias conditions.

Capacitance *	MIMOSA I		MIMOSA II		MIMOSA III	MIMOSA IV
	1 diode	4 diode	1 diode	2 diode		
Charge collecting diode	2.69 fF	10.76 fF	1.70 fF	3.40 fF	2.34 fF	2.10 fF
Reset transistor source-bulk diode	2.03 fF	2.03 fF	1.65 fF	1.65 fF	1.12 fF	1.94 fF
Interconnections + transistors parasitics	5.70 fF	12.38 fF	4.83 fF	4.59 fF	7.44 fF	6.66 fF
Total node capacitance (basic configuration in each chip)	10.42 fF	25.17 fF	8.18 fF	9.64 fF	10.90 fF	10.70 fF

Since pixels have a size of a few micrometers only, any direct method of measurement requiring an extra test circuitry, e.g. allowing injection of a test charge, becomes questionable. Such structures introduce parasitic capacitance, which can be comparable to the actual pixel capacitances and as a result affects the measured quantities. The following paragraphs show two calibration methods, which were successfully applied in characterisation of the fabricated MIMOSA prototypes. The first statistical approach is based on the Poisson statistics of shot noise [91]. This method uses the transfer curve, which is a plot of the square of the noise versus the mean signal resulting from charge integration over a specified time. The second method makes use of the photoelectric effect for soft X-rays. This method is commonly used for calibration of fully depleted detectors, where the carriers drift in the strong electric field towards collecting electrodes. However, it requires fully efficient charge collection in order to be precise. This assumption is justified in the case of fully depleted devices but has less meaning for MAPS devices, where the charge collection is achieved through thermal

* Values of junction capacitances are calculated for the reverse bias voltages of 3.2 V, 2.2 V, 1.7 V and 2.1 V for MIMOSA I, II, III and IV, respectively. These voltages result from estimated leakage currents according to the simulation models and the 400 ns long reset pulse signal with the repetition rate of 1.6 ms.

diffusion. Consequently, a new method for the calibration of MAPS devices was developed and is presented.

An example of a SPICE simulation aiming to estimate the charge-to-voltage gain as a function of the collected charge and the maximum signal range is shown in Figure 5-10, where the two pixel configurations from the MIMOSA I chip were examined. The maximum signal range is also called the full well capacity and is expressed in number of collected electrons. For the single diode configuration the full well capacity is close to 140×10^3 e^- and the charge-to voltage conversion gain varies between 14.6 $\mu V/e^-$ to 10.5 $\mu V/e^-$.

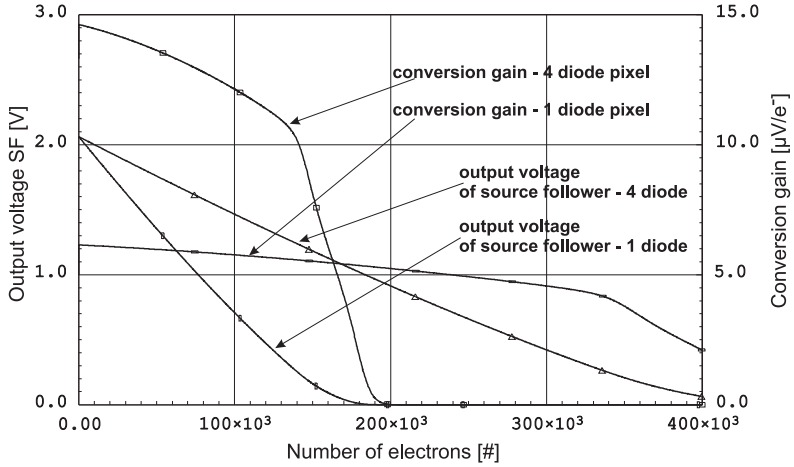

Figure 5-10: Charge-to-voltage conversion gain and corresponding voltage level at the output of an in-pixel source follower as a function of number of collected electrons for two pixels configurations.

In the case of the four-diode configuration the charge-to voltage conversion gain is much less and varies between 6.1 $\mu V/e^-$ to 4.9 $\mu V/e^-$, but the maximum signal range is more than two times larger than for the previous configuration.

5.3.2 Statistical Method of Calibration

The statistical method used for calibration exploits the Poisson statistics of the shot noise. To perform the calibration, the detector needs to be exposed to a variable photon flux, which can be a source of visible light and the flux variability can be achieved by varying the light intensity or the integration time. The shot noise is measured in this method as a variance of discrete samples of signal obtained in signal integration with a defined constant time period. The light source does not need to be calibrated; it should only be tuneable and feature good stability during the experiment. Both conditions are satisfied by any light-

emitting diode (LED), whose light intensity is controllable by the conveyed current. The current can be delivered by a high precision current source, thus the option based on the constant time period for integration of the photoelectron current was chosen for the MAPS calibration. The integration time can be equal to the read-out time of a single image frame*, and the integrated signal can be determined as the difference in amplitudes of two sequential frames, thus the integration time can be determined precisely. Actually, the value of the conversion rate can be obtained in two ways, i.e. using only one illumination level for which the ratio of the square of the signal variance and the mean value is derived or from the linear fit to the transfer curve, which is a plot of signal variance versus the mean signal obtained for some number of illumination intensities.

The collected charge during the integration time is given by

$$N_e = \eta\Phi, \tag{5-9}$$

where η is the quantum efficiency of the detector, defined as the number of photoelectrons per incident photon, and Φ is the number of photons incident during the integration time. If a detector is of sufficiently high quality that photon shot noise dominates over detector noise, the charge-to-voltage conversion gain can be determined by using the fact that shot noise obeys the Poisson distribution. A fluctuation σ_{phot} in a measured detector signal V_s is caused by a fluctuation in the number of detected photons $\sigma_{\eta\Phi}$. Thus it can be written as

$$\sigma_{phot} = \frac{\partial V_s}{\partial(\eta\Phi)}\sigma_{\eta\Phi} = G_{q\to V}\sigma_{\eta\Phi}. \tag{5-10}$$

For a Poisson distribution the standard deviation is the square root of the mean value. Therefore, assuming the average fluctuation to be the standard deviation, it is expressed by

$$\overline{\eta\Phi} = \frac{\overline{V_s}}{G_{q\to V}} \quad \text{and} \quad \sigma_{phot} = G_{q\to V}\sqrt{\overline{\eta\Phi}}. \tag{5-11}$$

Combining equations (5-10) and (5-11) yields the result allowing determination of the charge-to-voltage conversion from the experimental data obtained for a single detector illumination

$$G_{q\to V} = \frac{\sigma_{phot}^2}{\overline{V_s}}. \tag{5-12}$$

* Read-out time of a single image frame is defined for a sake of reference as a time required to address successively all pixels for a serial read-out starting from the first pixel and to the last one in an array of pixel in a MIMOSA-like detector.

For a detector working at the photon noise limit, calculating the charge-to-voltage conversion gain is fairly simple. The mean signal, $\overline{V_s}$, is easily calculated, and the sample variance is estimated from

$$\sigma_{phot}^2 = \frac{1}{N-1}\sum_{i=1}^{N}\left(V_{s,i} - \overline{V_s}\right), \tag{5-13}$$

where N is the number of samples taken.

Limiting the measurement to one individual illumination level allows a straightforward estimation of the charge-to-voltage conversion gain. Repeating calculations for several illumination levels allows to examine the conversion gain as a function of the signal height. This procedure is particularly important for devices exhibiting a significant degree of non-linearity of their response as a function of a measured signal level. Correspondingly, assuming that the charge-to-voltage conversion gain is independent of the signal magnitude, the plot of the signal variance as a function of the mean signal can be used to determine the actual value of this coefficient. The use of the transfer curves, rather than single illumination measurements, is justified for practical reasons, since it allows accounting for an irreducible read-out noise and provides immunity of the method to measurement errors. The capacitance, on which the charge to voltage conversion is realised, is a combination of the linear term and a sum of non-linear junction capacitances. The linear term usually dominates and for the practical use, the non-linearity is considered as a second order effect, and was neglected at a current stage of the MIMOSA chips performance evaluation.

In the MAPS detectors, there are two main independent sources of shot noise i.e. noise associated with the diode leakage current and the variation of the current due to the photon flux. Both shot noise contributions and remaining temporal noise sources not removed by subtraction of signals show up as a variation of the integrated charge. Thus, the variation σ, of the measured signal is a quadratic sum of three independent components

$$\sigma^2 = \sigma_{leak}^2 + \sigma_{phot}^2 + \sigma_n^2, \tag{5-14}$$

where σ_{leak}^2 and σ_{phot}^2 are fluctuations of the charge due to the leakage current and illumination. According to Poisson statistics, both terms are equal to the number of accumulated electrons. The last symbol σ_n^2 stands for the remaining read-out noise after subtraction of two acquired frames, and does not depends on the absorbed light intensity.

Since the measured voltage signal V_s is a sum of contributions due to the leakage current and the conversion of photons, the variance of the signal can be expressed by

$$\sigma^2\left(V_s\right) = G_{q\to V,SF} A_{read} V_s + \sigma_n^2 , \tag{5-15}$$

where A_{read} represents the total read-out gain. Thus, the charge-to-voltage gain is obtained by the slope of the linear fit to the experimental data, and in addition to the charge-to-voltage conversion gain, the irreducible electronic noise σ_n is determined by the square root of the intercept with the vertical axis. The transfer curve plot $\sigma^2\left(\overline{V_s}\right)$ is used for this purpose with the squared variance and the mean signal put on the abscissa axis and on the axis of ordinates, respectively.

5.3.3 Calibration with Low Energy X-Ray Photons

Alternatively to the statistical method, a radioactive source delivering low energy X-ray photons can be used for the calibration of the MAPS detectors. The energy of the photons should be chosen in such a way, that their attenuation length was compatible with the thickness of the active detector volume, and they could not be absorbed by the surface metal and passivation layers. For the calibration of the MIMOSA chips a ^{55}Fe radioactive source* was chosen. For 5.9 keV photons emitted from this source, a constant number of charge carriers about 1640 e-h pairs are created in silicon. The generated charge carriers give rise to a characteristic peak in the signal amplitude distribution. For detectors having intrinsic charge collection efficiency close to 100%, the position of this peak can be directly used for measurements of the conversion gain. The latter is not the case for the MAPS devices, where the charge is naturally spread among several pixels, and in average the charge collection is only partial. However, fully efficient charge collection takes place for photons converting inside the depleted volume of a p-n junction of the charge collecting diode. The high electric field present in the depletion zone separates rapidly the carries before they recombine, and transports the electrons onto the charge-sensing node. The full charge collection is also achieved for photons converting inside the shallow, not depleted n-type volume of the diode. In this case, the potential profile attracts electrons towards the shallow regions of the n^+-type

* The ^{55}Fe source delivers photons from two dominating γ emission modes i.e. Mn K_α 5.9 keV and Mn K_β 6.49 keV photons.

implants present in each diode to form the ohmic contacts. The electrons get blocked on the charge-sensing node. However, the holes, for which the potential profile is inversed with respect to the electrons, may diffuse towards the depletion zone of the diode where they are extracted and injected into the epitaxial layer. A weak electric field is present inside the n-well which results from the decreasing donor concentration with increasing n-type implant depth. Thus, the electric field intensifies movements of holes in the n-type zone of the charge collecting diode. Both groups of photons for which charge collection achieves 100% represent only a small sub-sample of the total flux incident on the detector. Charge generation process due to conversion of X-ray photons inside an active volume of a MAPS detector is illustrated in Figure 5-11, where two locations of photon conversions are shown. The charge liberated deeply in the detector volume is spread among neighbouring pixels and is partially lost due to diffusion far from the interaction point and due to recombination before collection. The signal on a single pixel is observed as a vast peak in the energy spectra. To some extent, summing signals from neighbouring pixels can improve the resolution of the peak and the resulting signal approaches whole generated charge. Nevertheless, due to inevitable and large charge losses, the charge-to-voltage calibration cannot be obtained from this peak.

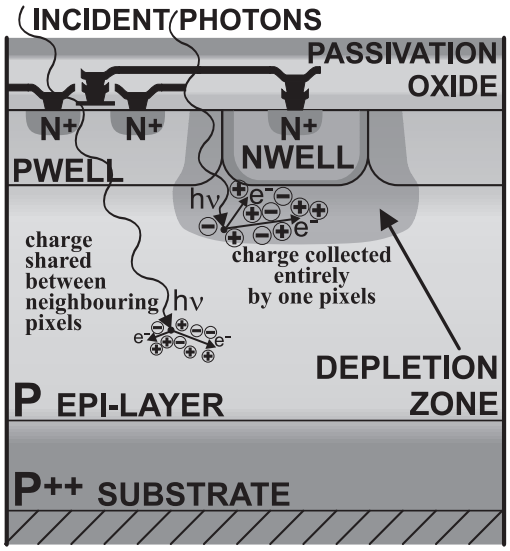

Figure 5-11: Conversion via photo-electric effect of an X-ray photon inside an active volume of a MAPS detector.

Additionally the possibility of improving the resolution by summing signals from the

neighbouring pixels is limited, due to the fact that starting from a given cluster multiplicity the SNR for the obtained cluster commence to deteriorate or explicitly the dominant contribution in the summed signal turns into noise. On the other hand, the charge released inside the charge collecting diode and in its vicinity is collected rapidly and with a full efficiency. This should give rise to the second, smaller peak distinguishable in the central pixel photon spectrum. Detailed simulations using the ISE-TCAD package were carried out in order to validate the proposed idea as a new method of the charge-to-voltage conversion gain calibration applicable to the MAPS devices. The combination of 4225 randomly chosen spatial positions of photon conversions in the two-dimensionally modelled MAPS detector was examined. The distribution of the number of simulation points as a function of the distance from the detector surface was chosen according to the exponential law of photon flux attenuation. Conversely, the lateral distribution of random points was uniform and restricted to the area of the central pixel only. The simplified two-dimensional model of the detector was chosen to speed up the simulation, since larger statistics was required to have a reliable conclusion from the simulation. The *heavy-ion* ionisation model, as described in Appendix-B, was chosen to simulate the point-like charge deposition of 5.9 keV photons emitted by a ^{55}Fe source. The signals were calculated for the central pixel only. The two-dimensional simulation of the charge collection of the single diode pixel configuration of pixel pitch of 20 μm and an epitaxial layer thickness of 15 μm are shown in Figure 5-12. The pulse height distribution in this figure is shown for signals detected on the central pixel only.

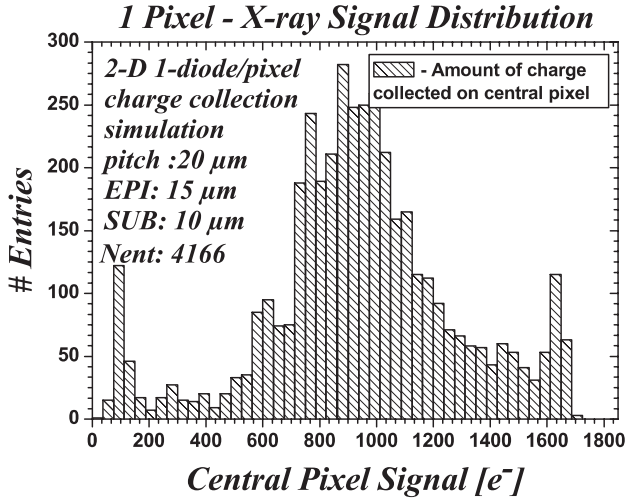

Figure 5-12: Pulse height distribution obtained in two-dimensional simulation of charge collection in one diode configuration of pixel pitch of 20 μm and an epitaxial layer thickness of 15 μm.

Apart of the wide peak placed at smaller amplitudes, which contains most entries, there is a second much narrower peak at high amplitude*. Thorough analysis shows that no charge is collected in the adjacent pixels for events in the second peak. Consequently, Figure 5-13 shows the spatial correlation between the position of the photon interaction point and the height of the estimated signal found in simulation. The highest signals arise from conversion points at the closest distance to the diode, positioned at the spatial co-ordinates (10,0) in this figure. The results of a two-dimensional simulation can only be qualitatively interpreted for a pixel detector. The two-dimensional structure is infinitive in the third dimension, resulting in a strip-like form of the detector. Generally, quantities, like the collected charge and the ratio between the numbers of entries in both peaks of the histogram, are affected by the particular geometry of the detector.

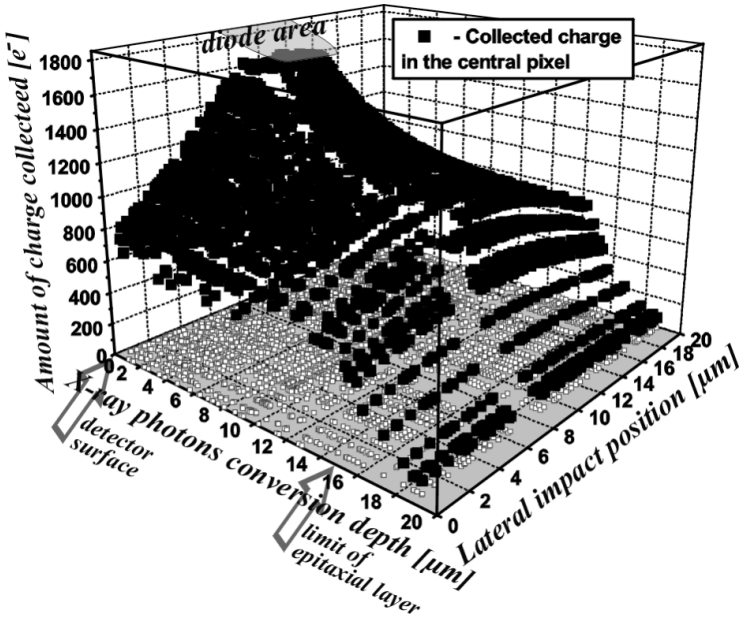

Figure 5-13: Correlation between the spatial position of the photon interaction point and the amount of the collected charge measured on the central pixel.

However, the presence of the second peak justifies the hypothesis on full charge collection for some subset of events. The position of the second, small peak can be used to measure the conversion gain and as a consequence other basic electrical parameters of the MAPS devices can be derived. The width of this characteristic second peak has its origin in the

* Another peak placed below 200 e^- in Figure 5-12 results from charge collection due to photons converting below epitaxial layer. In practice, this peak extends towards zero and enters into noise. In the simulation, the maximum depth reached by photons was limited to 20 µm, thus the signal spectrum was cut.

irreducible pixel read-out noise. For the high number of entries into the signal histogram, the precise value for the charge-to-voltage gain and the noise level can be estimated from the mean signal position and the width of the distribution, respectively.

5.4 Noise Performance

5.4.1 Temporal Noise

During the whole procedure of design, fabrication, and characterization of MAPS detectors, noise is always one of the most important parameters to be considered. Temporal noise is the temporal variation in pixel output values when the input does not undergo any changes. This noise sets the fundamental limit in sensor dynamic range, and reduces the sensor SNR*. In imaging application the noise effect is most pronounced at low illumination levels. Since the MAPS device, operated as a particle detector, is similar to the image sensor exposed to low illumination, it is SNR, instead of absolute noise that directly affects the detection performance. There are many sources of temporal noise in MAPS detector. It includes three major types of noise, namely thermal noise, shot noise, and flicker noise. Variance of the measured signal is often used to estimate the noise power. Shot noise occurs when dark current electrons pass through the diode. Additional noise is added when resetting the diode to the reverse bias and when reading out the pixel value. Other sources of noise include quantization noise showing up if the output analogue signal is to be digitised, coupling noise due to power supply fluctuation and substrate coupling from peripheral mainly digital circuits. The environmental interferences such as temperature variation, electromagnetic fields, and etc. can also cause the fluctuation in the sensor output, and thus cause the temporal noise. Some of the noise can be minimised by good circuit design practice. For example, applying appropriate layout techniques e.g. carefully implementing guard-rings and power supply lines distribution can reduce substrate noise. The intrinsic noise usually is hard to suppress, and results from the physics of the integrated circuit devices.

The general noise analysis is complicated by the nonlinearities in the charge-to-voltage

* The reduction in SNR is especially important under low light conditions, thus high end imaging applications usually have abandoned CMOS sensors so far. In imaging applications, temporal noise performance of CMOS image sensors still lag behind CCD image sensors.

conversion and in the reset transistor. The rigorous noise analysis requires taking into consideration the non-stationary character of the circuit models and the non-stationary character of noise sources including 1/f noise, i.e. the dependence of circuit representation on time resulting from switching operation. The non-linearity of the collected charge to voltage conversion is also required to be considered in the analysis. This kind of analysis is necessary for example for the full study of the reset operation and one approach can be found in [92].

For the call of this work, only the standard noise analysis has been carried out as sufficient for correct interpretation of the experimental results [93]. The noise analysis must be done separately for the three phases of operation, i.e. reset, integration and read-out. Noise generated during read-out is directly computed at the output node, while noise generated during reset and integration is sampled onto C_{conv} first, and then transferred to the output during read-out. In the experimental results presented in this work, the CDS signal processing has been consistently used by off-line subtraction of subsequent frames. The use of CDS is beneficial in the reduction of the overall noise for several reasons. First, it removes the reset noise, which is usually the dominant source of temporal noise. Secondly, it reduces the influence of the low-frequency noise, mainly 1/f noise, compensates for external couplings added in the same phase to the both signal samples and allows to make pixel response uniform by removing spatial dispersion of pixel output levels derived from non-uniformity in the array usually called Fixed Pattern Noise, FPN. The schematic diagram of a single pixel with the simplified read-out chain is presented in Figure 5-14. The pixel in the active array is selected by activating row (*ROW_SEL*) and column (*COL_SEL*) addressing lines. The bias current of the transistor M4 is switched to the source follower transistor M2 and the amplified signal corresponding to the diode voltage is available at the output node for the data acquisition system. The CDS signal processing is represented in Figure 5-14 by the delay with time constant τ and a block realising signal summation. The transfer function of CDS falls to zero at low frequency and is given by

$$\left|H_{CDS}(f)\right|^2 = \left|1 - e^{-2j\pi f\tau}\right|^2 = 4\,\mathbf{sin}^2(\pi f\tau). \tag{5-16}$$

The characteristic of the read-out chain is practically reduced to the first order low-pass filter, since the source follower as the slowest component determines frequency behaviour of the read-out in the system. Including low-pass characteristic of the read-out channel with cut-off

frequency f_{3dB} the squared modulus of the CDS transfer function represents pass-band characteristic and is given by

$$\left|H_{CDS,LP}(f)\right|^2 = \frac{4f_{3dB}^2 \sin^2(\pi f\tau)}{f^2 + f_{3dB}^2}. \tag{5-17}$$

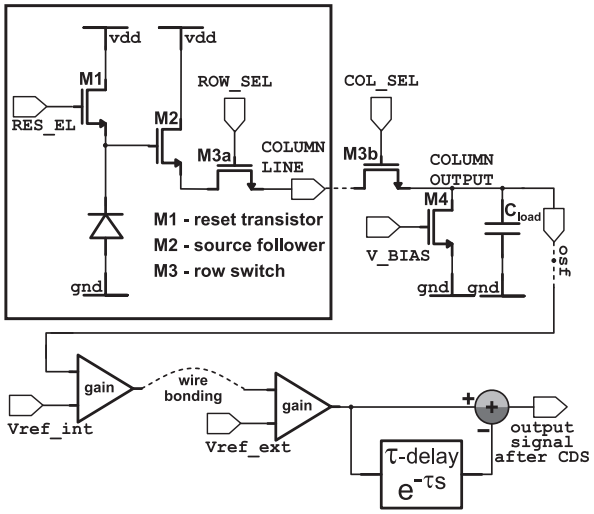

Figure 5-14: Single pixel architecture with simplified model of a read-out and signal processing chain.

5.4.1.1 Noise During Reset

Periodically, the floating diffusion of the collecting diode has to be reset to remove the collected charge and to compensate the diode leakage current. In practical applications, the reset operation is repeated few times per second in order to avoid the saturation of the diode due to the leakage current. The minimum reset frequency depends on the exact value of the leakage current, which in turn is a steep function of the operating temperature. During the reset, the transistor M3 in Figure 5-14 is turned off and a positive voltage pulse is applied to the gate of M1. At the beginning of reset, the latter is saturated, biased in a strong inversion or in the sub-threshold depending on the voltage established on the diode at the end of integration. If this voltage is low, M1 is in strong inversion first and for a very short time, and then it enters weak inversion for the rest of the reset phase. If the duration of the reset pulse is equal or grater than the time needed for the drain current of the reset transistor to draw its level to the dark current of the diode, the steady state is achieved. The average reset noise power can be calculated in this case by means of the commonly known expression describing thermodynamic fluctuations

$$\overline{V_{n,res}^2} = \frac{kT}{C_{conv}}. \tag{5-18}$$

However in real systems the steady state is rarely obtained, because of the insufficient duration of the reset phase. It can be shown [94, 92] that in this case, the average reset noise power is close to

$$\overline{V_{n,res}^2} = \frac{1}{2}\frac{kT}{C_{conv}}. \tag{5-19}$$

Reset noise, expressed in equivalent noise charge can be as high as few tens of electrons and it is the dominant contribution to the total noise. Fortunately, kTC noise is removed applying the CDS technique. The price to pay is an increase of the white noise contribution, since the positive signal correlation occurs only at multiples of the frequency, which is the inverse of the delay time of the CDS filter.

5.4.1.2 Noise During Integration

The dominant noise source during the integration phase is the shot noise due to the diode leakage current i_{leak}. At room temperature the mean value of this current is in the typical MAPS design in the order of maximum several femtoamperes, and the related noise contribution is not significant for practically used integration time values up to a few milliseconds. This type of noise should be taken into account when the integration time increases or for irradiated circuits affected by the increase of leakage currents. More precise analysis should also include the change of the diode capacitance during the charge integration. The latter is a second order effect and is neglected for the same reasons as it was done before in the case of charge-to-voltage conversion gain estimation in Chapter 5.3.1. The mean square value of the noise sampled on the conversion capacitance at the end of the integration time t_{int} is given by

$$\overline{V_{n,int}^2} = \frac{q\, i_{leak}}{C_{conv}^2} t_{int}. \tag{5-20}$$

5.4.1.3 Noise During Read-out

During read-out, the transistors M2, M3 as well as the column switches M3a and M3b and the source follower current source M4 are the noise sources. The remaining column and

chip level circuitry is neglected in the noise analysis, since their noise contribution does not yield the dominant noise.

The read-out noise can be easily calculated via the small signal representation of the circuit shown in Figure 5-14. For the AC small signal, the gate of the source follower transistor is floating. This fact results in an equivalent input resistance seen from the source of M2, depending for small an medium frequencies on the ratio of two capacitances and is given by

$$Z_{eq} = \frac{1+m}{m\, g_{m,M2}}, \text{ where } m = \frac{C_{conv}}{C_{gs,M2}}. \tag{5-21}$$

Integrating over the frequency band and using noise definitions introduced in Chapter 3.2.4, the output-referred thermal mean square noise voltages due to component transistors without CDS processing are expressed by:

$$\overline{V_{n,M2}^2} = \frac{nkT\gamma}{C_L} \frac{(1+m)^2}{m\left(1+m\left(1+g_{m,M2}\left(r_{ds,M3a}+r_{ds,M3b}\right)\right)\right)}, \tag{5-22}$$

$$\overline{V_{n,M3a}^2} = \frac{kT}{C_L} \frac{m\, g_{m,M2} r_{ds,M3a}}{\left(1+m\left(m\, g_{m,M2}\left(r_{ds,M3a}+r_{ds,M3b}\right)\right)\right)}, \tag{5-23}$$

$$\overline{V_{n,M3b}^2} = \frac{kT}{C_L} \frac{g_{m,M2} m \left(r_{ds,M3a}+r_{ds,M3b}\right)^2}{r_{ds,M3b}\left(1+m\left(1+g_{m,M2}\left(r_{ds,M3a}+r_{ds,M3b}\right)\right)\right)}, \tag{5-24}$$

$$V_{n,M4}^2 = \frac{nkT\gamma}{C_L} \frac{g_{m,M4}\left(1+m\left(1+g_{m,M2}\left(r_{ds,M3a}+r_{ds,M3b}\right)\right)\right)}{m g_{m,M2}}, \tag{5-25}$$

where $g_{m,Mx}$ and $r_{ds,Mx}$ are, respectively, the output transconductance and resistance of the transistor Mx. The channel resistances of M3a and M3b are usually low. After investigation of the above equations, it can be noticed that the noise due to M3a and M3b is at least several times lower than the noise due to M2 and M4. Additionally, taking the ratio of equations (5-22) and (5-25), which is given by

$$\frac{\overline{V_{n,M2}^2}}{\overline{V_{n,M4}^2}} = \frac{g_{m,M2}}{g_{m,M4}\left(1+g_{m,M2}\left(r_{ds,M3a}+r_{ds,M3b}\right)\right)^2}, \tag{5-26}$$

it becomes clear that if the transconductance of the current source can be made low, the source follower transistor dominates the output-referred noise voltage. The thermal noise is

not suppressed by CDS; it enters effectively in the measured noise. Its minimisation requires the reduced transconductance of the current source, which can be achieved by a choice of a small W/L ratio for this transistor. The increase of the capacitive load of the source follower by the capacitance C_L limits the bandwidth of the whole system and results in the noise power proportionally reduced. Thus, the loading capacitance is very important, and its value should be selected as high as possible allowing only correct signal rise-time at the output*. In practice, the rise time should be less than one read-out clock period, unless the read-out architecture with two lines switched alternatively to the output amplifier is used as shown in Figure 5-2b. In the case of MIMOSA II, an additional capacitance C=2.5 pF loading both read-out lines in the chip allowed to decrease the ENC value by 10% with regard to the initial value. At the same time, the transconductance of the source follower should be high for optimum noise performance. Both transconductances depend on the transistor dimensions and the bias current. The current source transistor M4 has no influence on the conversion gain. It is placed outside the pixel, and it can be optimised with more freedom reducing significantly its noise contribution to the total output noise. The choice of the W/L ratio for the current source is only constrained by the drain-to-source saturation voltage, whose increased value should not limit the voltage swing at the output of source follower. Whereas, the maximised W/L ratio of the source follower transistor is preferred. However, the total gate area should not exceed certain limits to keep high value of the charge-to-voltage conversion gain. For fixed transistor dimensions, the transconductance value can be increased applying higher bias current. Nevertheless, the bias current cannot be too high, because it implies the increased gate-to-source voltage of the source follower transistor limiting the voltage swing. Thus, the correct choice of parameters resulting in good noise detector performance includes the load capacitance C_L, the bias current and dimensions of the source follower and current source transistors. It is done aiming for the bandwidth allowing fast read-out and sufficiently large voltage swing.

Calculating the output-referred mean square flicker noise voltages is less explicit.

* The speed of a source follower built with an NMOS transistor is higher for rising signals. In this case, the transconducatnce of the source follower is modulated by a signal and the load capacitance is charged with a current whose value depends on the signal change. In the case of falling signal, the load capacitance is discharged with a constant limited current of the current source. In some practical implementations, the speed of a source follower is increased by adding a parallel switch to the load capacitance and applying short negative pulse discharging the capacitance before reading out the actual signal.

However, after some reduction and supposing the definite integral lower limit is much less than 1 Hz the source follower transistor contribution without CDS processing is given by

$$\overline{V_{n1/f,M2}^2} = \frac{K_F (1+m)^2}{2 C_{ox} L W m^2} \mathrm{Log}\left(\frac{g_{m,M2}^2 m^2}{4\pi^2 f_d^2 C_L^2 (1+m)^2} \right), \tag{5-27}$$

where f_d is a low frequency limit of integration over the flicker noise bandwidth.

The CDS processing was used as a technique for offset- and reset noise removal, both of which are associated with charge sensing circuits employed at each pixel. In this analysis a simplified continuous model of the CDS processing was used. The fold-over effects on the noise spectrum due to sampling that is applied in the data acquisition used in the experiment were neglected. Despite this simplification, the variance of the sampled signal remains unchanged with respect to the continuous signal processing shown in Figure 5-14. This approach allows using SPICE simulator to calculate the output-referred noise power density spectra. The use of SPICE allows to include transistor electrical parameters that are calculated precisely using advanced transistor models for the particular bias of the pixel circuit. The total pixel thermal and flicker noise power spectrum density before CDS can be estimated by fitting the SPICE simulated curves to the following expression

$$S(f) = S_0 \left(1 + \frac{f_c}{f} \right), \tag{5-28}$$

where $S(f)$ is the total spectral noise power density referred to the input of the source follower, S_0 is the fitting component and f_c is the flicker noise corner frequency. The noise spectral density $S_{CDS}(f)$ after CDS is a product of the noise power density and the transfer function given by (5-28) and (5-17), respectively

$$S_{CDS}(f) = S(f) \cdot \left| H_{CDS,LP}(f) \right|^2. \tag{5-29}$$

The CDS processing increases the contribution of white noise, and the ratio between the noise due to the source follower transistor before CDS (5-22) and after processing $\overline{V_{nCDS,M2}^2}$ is given by

$$\frac{\overline{V_{n,M2}^2}}{\overline{V_{nCDS,M2}^2}} = 2\left[1 - e^{\frac{-\tau m g_{m,M2}}{C_L\left(1+m\left(1+g_{m,M2}\left(r_{ds,M3a}+r_{ds,M3b}\right)\right)\right)}} \right]. \tag{5-30}$$

In the extreme case for a very long delay τ, the output-referred root mean square noise

(r.m.s.) is increased by factor $\sqrt{2}$. Figure 5-15 shows the output-referred noise power spectra at the output of the source follower before and after CDS processing for the MIMOSA I and II chips as a function of different CDS intervals equal to signal integration time values. In these plots flicker and thermal noise components are combined. Sampling frequencies of 0.625, 1.25, 2.5, 5 and 10 MHz were examined. The r.m.s. value of the ENC value depends on the DC voltage gain G_V of the read-out amplifier and on the charge-to-voltage conversion gain of the pixel $G_{q\to V,SF}$. The numerical values of the noise presented in this figure were obtained by a numerical integration of power spectral density distributions according to

$$\text{rmsNoise} = \frac{1}{G_{q\to V,SF} G_V} \sqrt{\int_{f_d}^{\infty} S_{out}(f)\ df}\,, \tag{5-31}$$

where $S_{out}(f)$ is the noise power spectral density.

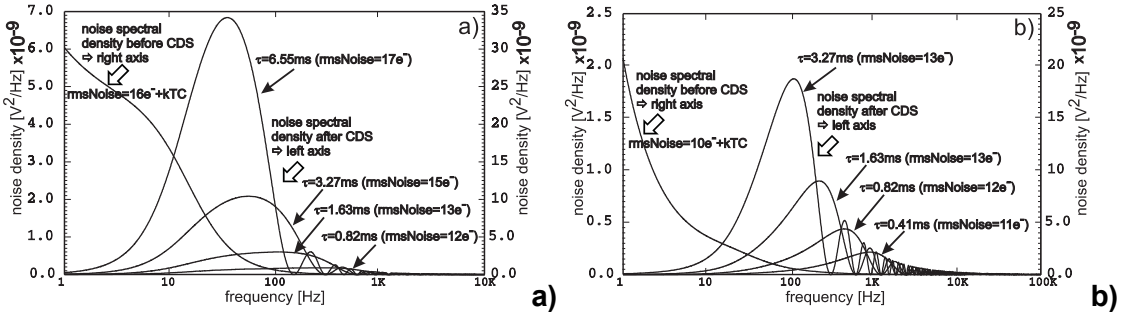

Figure 5-15: Output noise spectral densities before (right y-axis) and after (left y-axis) CDS processing for (a) MIMOSA I and (b) MIMOSA II.

The radiation tolerant design demands a compromise with respect to noise optimisation, since the dimensions of the transistors cannot be chosen freely. The main reason for a slightly worse noise performance is a lower value of the charge-to-voltage conversion gain due to parasitic gate capacitance of the source follower. The standard non-radiation tolerant design gives an ENC between 10% to 20% better than the design with all transistors enclosed.

The noise contribution of output amplifiers, designed with the input stage shown in Figure 5-5, was estimated to be below the noise level generated in the pixel. For the sake of reference, the r.m.s. noise value after CDS processing referred to the amplifier input was estimated to be 46 μV and 72 μV for MIMOSA I and II, respectively. Higher input noise in

the case of MIMOSA II is explained by a complementary rail-to-rail topology of the input stage used for the design of the off-pixel amplifier in this chip.

5.4.2 MIMOSA III, Noise Optimisation for 0.25 μm CMOS Process

The motivation for this work was to design the detector providing the best performance for future applications in terms of SNR, read-out speed, spatial resolution and radiation hardness In modern sub-micrometer processes, operation of a MOS transistor in strong inversion is only available under high bias currents, and what follows high gate-to-source voltages. The use of high bias voltages and currents is impractical, since the signal swing is drastically reduced and the total power consumption increases. Additionally, noise parameters of a MOS transistor operated in strong inversion, what is especially a case of an N-type device, are worse comparing to the device biased in moderate or weak inversion. In contrast, operation of a transistor in weak inversion increases signal swing, and in some applications is interesting from the noise point of view, but the speed is noticeably limited.

The design of the MIMOSA III chip has been implemented in a 0.25 μm commercial CMOS process, which features twin-tubs implanted into a 2.0 μm thick p-type epitaxial layer, nominal power supply voltage of 2.5 V, gate oxide thickness t_{ox}=5.84 nm, Shallow Trench Isolation (STI) and three interconnection metal layers. The expected mean signal from minimum ionising particles has been estimated around 150 of collected electrons on the seed pixel at room temperature. This estimation sums charges originating in the epitaxial layer and the substrate. While, according to the device simulation, it is assumed that effective thickness of 2.5 μm of the substrate contributes to the signal.

The noise performance of the detector can be improved by the use of the technique, which has already proved its efficiency for the previous prototypes, consisting in the read-out architecture with two readout lines switched alternatively to the output amplifier at the reduced bandwidth of the source follower. However, a detailed noise optimisation focused on the appropriate scaling of active devices was necessary. Taking into considerations the low signal expected in conjunction with a strong dependence of the generated noise in the transistors on their dimensions for the sub-micrometer process used, special attention was given to the source follower transistor. As a result of the noise analysis, the maximum value of the ratio of the charge-to-voltage conversion gain and the output noise r.m.s value were

estimated. In order to estimate precisely parasitic capacitances, affecting the charge-to-voltage conversion gain, transistors laid out with an enclosed gate form were requiring separate extraction of the drain and source geometrical parameters for each combination of their gate width and length. Thus, the optimisation procedure required to work on mask layouts, and to continuously repeat physical extraction for the drawn devices. Noise calculations were done using HSPICE simulator, which was imposed by the availability of transistor models. The charge-to-voltage conversion gain was determined after extraction of pixel layouts including parasitic capacitances of transistors, interconnecting lines and the n-well/p-epi diode. The parameters of the default noise models of MOS transistors implemented in HSPICE were updated to the values obtained experimentally for the considered fabrication process for transistors under different bias conditions and of different gate lengths[*]. This arduous work was carried out only for 28 different transistors at five, varying from weak to strong inversion, bias conditions. Figure 5-16 shows simulated characteristics $I_{DS}\left(V_{GS}\right)$ for the minimum gate width W of enclosed transistors in the source follower configuration simulated for increasingly changed values of the gate length L. The current range within the scope of this analysis was between $1\,\mu A$ and $50\,\mu A$. Higher current values were not considered, since they force transistor to operate deeper in strong inversion, limiting the output signal swing due to the increased V_{GS}.

The designed detector was equipped with a single analogue output, with the information from each pixel being read out with consecutive clock cycles of the readout clock addressing pixels. The detector operated in this mode is a charge-integrating device with an integration time equal to the readout time of one full frame. Thereby, due to the detector architecture, the integration time is equal to the CDS delay time τ. Because of that, the lower limit of this delay time is practically determined, since the read-out speed cannot be increased endlessly. The new detector has been foreseen to work with a read-out clock frequency of up to 40 MHz, with its default operation at 20 MHz. The total number of pixels in one array is 16384, that translates to $\tau = 820\,\mu s$ for the default clocking. The signal sample becomes available for read-out during a second clock cycle after switching on the bias current in the source follower transistor. Thanks to the alternating read-out, the source follower output has

[*] The detailed parameterisation of the considered 0.25 μm process for applications in high energy physics experiments was carried out at the Microelectronics Group at the CERN EP division within the frame of the RD-49 activity; http://rd49.web.cern.ch/RD49/welcome.html.

twice as long time to stabilise. For calculating the necessary bandwidth, the magnitude of the signal was assumed to be equal to the pixel-to-pixel DC level dispersion, which was expected around 100 mV. The bandwidth of the source follower results from the combination of the bias current, transistor dimensions and the loading capacitance. Its value was fixed for the read-out speed required and the loading capacitance was chosen adaptively to satisfy this condition for each combination of the source follower transistor dimensions and bias currents. As an optimisation criterion, the maximum value of the charge-to-voltage conversion gain to the total output-referred noise ratio was chosen.

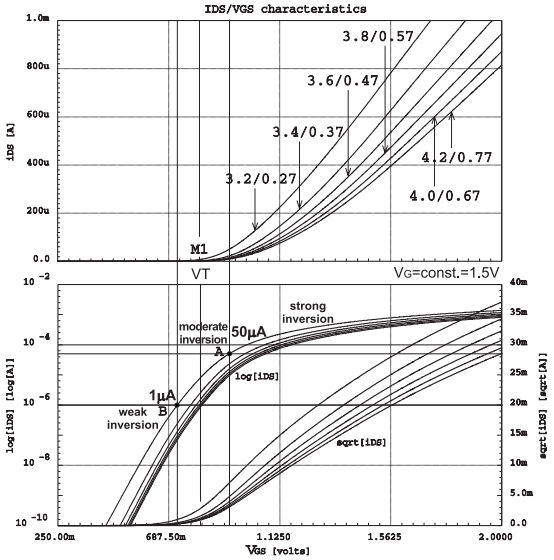

Figure 5-16: $I_{DS}\left(V_{GS}\right)$ characteristics for enclosed transistors of minimum channel width W for increasing values of gate lenght L.

The results of the optimisation procedure are presented in Figure 5-17. This figure shows data for transistors of different gate lengths and the minimum width corresponding to the particular gate length. Three subplots present results obtained for three different bias currents. The optimum bias current resulting in the optimum noise performance and providing reasonable output voltage swing about 400 mV is about 20 µA. Taking into account only the source follower contribution to the total noise, the optimum gate length lies between 0.45 µm and 0.75 µm, which are much higher than 0.25 µm of the minimum gate length available for the process. Finally, after the noise components for the remaining transistors were included, the source follower transistor with the gate length of 0.47 µm was chosen. The width of the transistor was set to 3.6 µm, which was the minimum width

obtainable for the gate length chosen. The charge-to-voltage conversion gain for this pixel configuration was calculated to be about 13.1 μV/e-. It is apparent that the curves in Figure 5-17 bend for short gates. The maximum present in the plots results from the increased contribution of the flicker noise, which dominates the maximum of the charge-to-voltage conversion gain value achieved for the smallest gate area of the source follower transistor. The noise optimisation yielded in the approximate input-referred noise of 6 e^- ENC for the MIMOSA III design. This value needed to be confirmed in measurements.

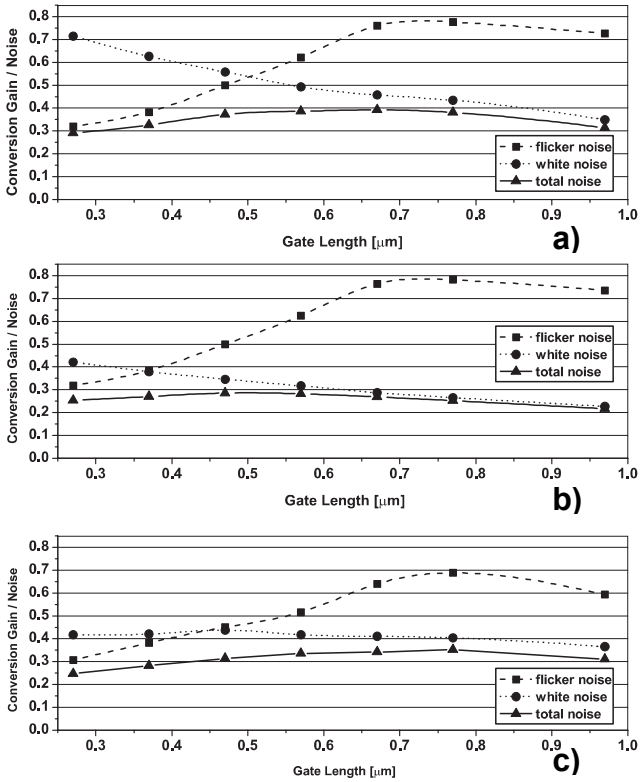

Figure 5-17: Ratio of the charge-to-voltage conversion gain to the total output-referred noise for the (a) optimum 20 μA current, (b) 5 μA and (c) 50 μA.

Figure 5-18a and Figure 5-18b show noise power densities referred to the output of the source follower after CDS processing. In these plots flicker and thermal noise components are shown separately and the total noise power spectrum can be calculated as a sum of these two curves.

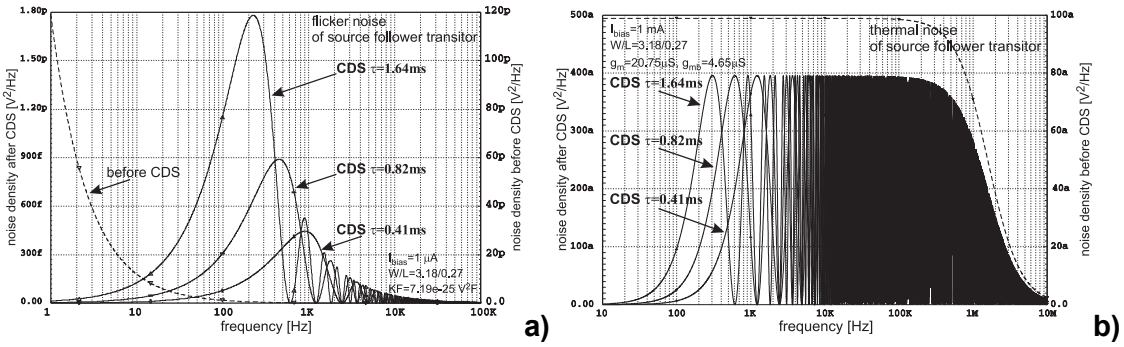

Figure 5-18: Output referred (a) flicker and (b) thermal noise power spectral density after CDS.

Table 5-12 gives summary of total ENC, estimated for different configurations of the MIMOSA chips obtained for typical read-out frequencies. The quoted frequency values were then used in tests of chips allowing referencing the measured values to the simulated ones. The typical noise charge amounts to a dozen or so electrons, and the full range extends from 6 e^- to 32 e^-.

Table 5-12: ENC estimated for the MIMOSA chips for typical read-out frequencies used in tests.

	MIMOSA I		MIMOSA II (rad-tolerant layout)		MIMOSA III	MIMOSA IV
	1-diode	4-diode	1-diode	2-diode		
Equivalent Noise Charge ENC	15 e^- @ 1.25 MHz	32 e^- @ 1.25 MHz	13 e^- @ 2.5 MHz	17 e^- @ 2.5 MHz	6 e^- @ 20 MHz	9 e^- @ 10 MHz

5.5 Influence of Reset Dynamics on Pixel Performance

The discussion presented in this paragraph aims to find the proper voltages during reset on the pixel diode as a function of time. The analysis has been carried out for the MIMOSA I chip and the parameters of a 0.6 μm CMOS fabrication process were employed directly into the equations and the derived formulas. This approach allows to simplify formulas, which would be difficult to derive in a full analytical form. However, the method used is general and similar results can be derived for other processes.

When reset begins with the discharged state of the conversion capacitance C_{conv}, the diode voltage $V_d(t)$ follows differential equation

$$\frac{dV_d(t)}{dt} - \frac{1}{C_{conv}}\left(I_{DS,SAT}(t) - I_{leak}\right) = 0, \tag{5-32}$$

with the initial condition given by

$$V_d(0) = V_{bi} = 0.84\ \text{V}, \tag{5-33}$$

where $I_{DS,SAT}(t)$ is the drain-source current of the reset transistor and V_{bi} is a diode built-in potential. At the beginning of reset, the diode leakage current can be neglected, because it is orders of magnitude less than the reset transistor current. However, the current that is conveyed by the reset transistor decreases in time. The conversion capacitance is being charged through the reset transistor, and as the charge stored on this capacitance increases the gate-to-source voltage of the reset transistor decreases. The dependence of the $I_{DS,SAT}(t)$ current on the reset transistor size through the ratio W/L, power supply V_{dd} and the diode voltage $V_d(t)$ is given according to the following formula

$$\begin{cases} I_{DS,SAT} = \dfrac{1}{2}\beta\dfrac{W}{L}\left(V_{dd} - V_d(t) - V_T(t)\right)^2, \quad \text{where} \\ V_T(t) = V_{T0} + \gamma\left(\sqrt{V_d(t) + 2|\varphi_F|} - \sqrt{2|\varphi_F|}\right) \\ \beta = \dfrac{\mu_n}{C_{ox}}\dfrac{W}{L}, \quad \gamma = \dfrac{\sqrt{2\varepsilon_{Si}qN_{SUB}}}{C_{ox}}, \quad \varphi_F = \dfrac{kT}{q}\ln\left(\dfrac{N_{SUB}}{n_i}\right), \text{and} \end{cases} \tag{5-34}$$

N_{SUB} is the substrate doping. Introducing numerical values for process parameters into equation (5-34), it results in the simplified expressions:

$$\begin{cases} I_{DS,SAT} = 54.5\times10^{-6}\dfrac{W}{L}\left(V_{dd} - V_d(t) - V_T(t)\right)^2 \\ V_T(t) = 0.89 + 0.65\left(\sqrt{V_d(t) + 0.81} - 0.90\right) \end{cases}. \tag{5-35}$$

For some time after beginning of reset, the reset transistor operates above threshold. The gate-to-source voltage for which the transition from the region of strong inversion to weak inversion characteristic of the device occurs is designated as $V_{ON}(t)$. The transition voltage $V_{ON}(t)$ is greater than $V_T(t)$, and is given by

$$V_{ON}(t) = V_T(t) + \frac{kT}{q}n(t) = V_T(t) + \frac{kT}{q}\left(1 + \frac{\gamma}{2\sqrt{2|\varphi_F| + V_d(t)}}\right), \tag{5-36}$$

which after substituting of numerical values results in

$$V_{ON}(t) = V_T(t) + 0.025 + \frac{0.017}{\sqrt{4V_d(t) + 3.24}}. \quad (5\text{-}37)$$

The analytical solution for the equation (5-32) as a function of time, the ratio W/L and the conversion capacitance C_{conv} can be derived expanding equation (5-34) in Taylor's series about the point $V_{dd} - V_d(t) = V_{ON}(t)$. The leakage current I_{leak}, due to its incommensurably low value with respect to the reset transistor current can be neglected, and the solution for $V_d(t)$ at V_{dd}=5 V is given by

$$V_d(t) = 3.366 - 0.558\times10^{-3}\left[\arctan\left(6028.2 - 1790.6V_d(0)\right) - \tan\frac{4.094\times10^{-8}}{C_{conv}}\frac{W}{L}t\right] \quad (5\text{-}38)$$

When the initial condition (5-33) is applied, equation (5-38) takes on a simply form

$$V_d(t) = 3.366 - 0.558\times10^{-3}\left[1.571 - \tan\frac{4.094\times10^{-8}}{C_{conv}}\frac{W}{L}t\right]. \quad (5\text{-}39)$$

In this simplified analysis, the transition voltage V_{ON} does not depend on transistor dimensions. Its value is close to 1.65 V and the corresponding voltage on the conversion capacitance amounts to about 3.35 V. The time needed to the voltage on the conversion capacitance to reach the transition point is very short. Even for a small W/L ratio for the reset transistor and typical values of the conversion capacitance, the transition state is achieved within a few nanoseconds after initiating the reset phase. This effect is illustrated in Figure 5-19 showing the increase of the voltage resulting from resetting the conversion capacitance for three dimensions of the reset transistor operated above threshold.

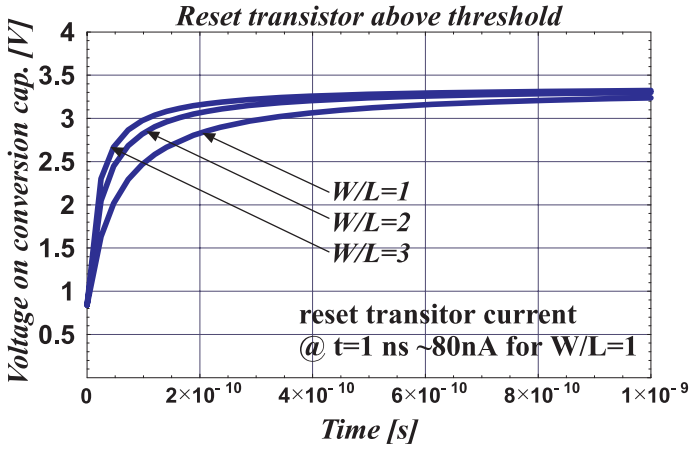

Figure 5-19: Reset voltage increase for reset transistor operating above threshold.

The current conveyed by the reset transistor at the transition point scales decreasingly with its W/L ratio, and is usually much below 1 μA. For the considered process, the reset transistor current at the transition point is given by the approximate expression $5.187\times10^{-8}\ \mathrm{W/L}$, and the time at which this transition occurs depends on the conversion capacitance and amounts to $0.507\times10^{6}\,C_{conv}\left(\mathrm{W/L}\right)^{-1}$. The transition current is still much higher than practically experienced leakage currents in the pixel, and the process of charging the pixel capacitance may still be continued.

Beyond transition, the reset operation is still continued, but the current of the reset transistor is significantly decreased. In order to continue the analysis for the reset transistor operated in sub-threshold, the leakage current of the diode in the differential equation (5-32) must not be eliminated.

For most of the reset time, the reset transistor operates in sub-threshold and, the drain current can be expressed by [95]

$$I_{DS}^{SUB}(t)=\frac{W}{L}I_0 e^{\left[\frac{(V_{gr}-V_d(t))q}{n(t)kT}-\frac{(V_d(t)-V_{br})q\left(1-1/n(t)\right)}{kT}\right]}\left(1-e^{-\frac{(V_{dr}-V_d(t))q}{kT}}\right). \tag{5-40}$$

The expression (5-40), after introducing process parameters and after some rearrangements, simplifies to the form

$$I_{DS}^{SUB}(t)=I_0\frac{W}{L}e^{\frac{40(5-V_d(t))}{n(t)}-40\left(1-\frac{1}{n(t)}\right)V_d(t)}, \tag{5-41}$$

where the gate efficiency parameter n is given by

$$n(t)=1+\frac{0.68}{\sqrt{4V_d(t)+3.24}}. \tag{5-42}$$

The most important variation of the voltage on the conversion capacitance falls on the part of reset for which the reset transistor is above threshold. During the second phase, this voltage changes only slightly. Therefore, it hardly influences the gate efficiency parameter n. For the sake of simplicity of the remaining computations, its average value $n_{av}=\left(n(V_{ON})+n(V_{dd})\right)/2$ was introduced into equation (5-41).

The differential equation (5-32), with the new initial condition $V_d(0)=V_{dd}-V_{ON}=3.45\ \mathrm{V}$,

yields the solution

$$V_d(t) = 2.922 + 0.025 \ln\left[\frac{1}{I_{leak}} e^{-40\frac{I_{leak}}{C_{conv}} t\left(1.937\times10^7 I_{leak} - \frac{W}{L}\right) + \frac{W}{L}}\right]. \quad (5\text{-}43)$$

A leakage current of the diode depends on the diode dimensions and temperature. It determines the steady state achieved at the end of the reset operation. Figure 5-20 shows the voltage increase on the conversion capacitance for the reset transistor operated below threshold as a function of time for different leakage currents. The typical value of the leakage current for the minimum size charge collecting diode at 300 K is in the order of a few femtoamperes. Thus, taking as an example 1 fA leakage current, the steady state is achieved after the settle time as long as hundred of milliseconds. In practice, when the reset pulse has a maximum length of several read-out clock pulses, the steady state is never achieved or it occurs in number of reset operations. On the other hand, for high leakage currents or for an exposure to the constant fluxes e.g. visible photons, the steady state is achieved in a short time*. The reset voltage is yet lower in this case.

The voltage on the conversion capacitance at the end of the reset operation depends on the reset time and the initial voltage. This effect gives rise to variations of the pixel output level observed in following read-out operations. These variations can be much higher than signal variance due to the presence of reset noise. The special case, where high variation can be observed, is the operation mode of the detector when reset operations are performed in irregular time intervals. In practice this mode is used in a system exploiting a randomly distributed in time trigger signals, which are delivered from outside and associated to events to be registered. If the reset operation is performed after each accepted trigger in such a system, different time pending the reset operation results in different initial voltages. Fortunately, similarly to the kTC noise, this effect does not introduce any temporal fluctuations during read-out and can be eliminated using CDS processing. However, the incomplete reset makes difficult operation of a detector, in which the recent signal sample is compared with the reference value resulted from measurements separated by reset operations performed in different time slots.

* The method of achieving steady state in a short reset time is to bias the reset transistor in a linear region. The method is know in visible light applications as a hard reset. The limitation of this method is significantly smaller voltage on the conversion capacitance after the reset operation and the reset noise featuring the full kTC value of the reset noise.

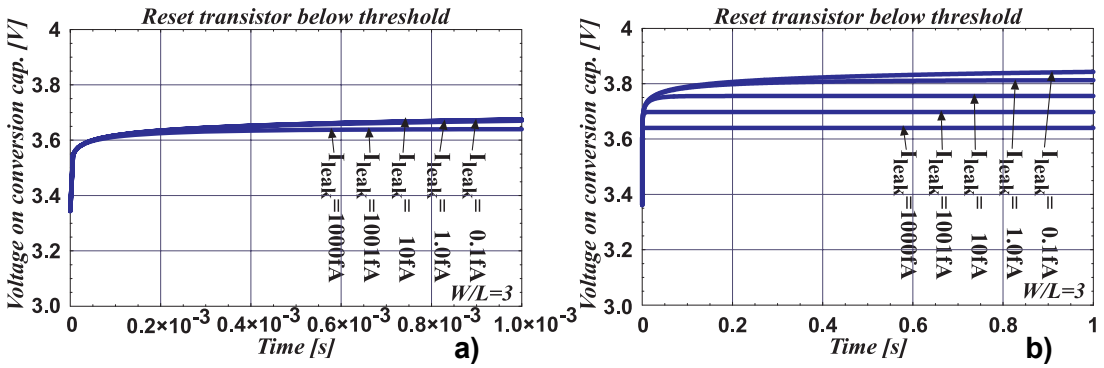

Figure 5-20: Reset voltage increase for reset transistor operating below threshold (a) for the first millisecond, and (b) for the first second of the reset phase.

Special care is required to provide signal swing matched with possible variation of the voltage level due to the incomplete reset operation. This requirement is important for systems with MAPS detectors, where the raw data are transmitted and all data processing is done in the external circuitry or off-line, in software.

Chapter 6

MEASUREMENTS OF THE PROTOTYPE PIXEL DEVICES

6.1 Introduction

The prototype MAPS devices were tested to validate their usefulness for future application in high energy and nuclear physics applications, where charged particle imaging is required. The programme-included verification of basic electrical parameters, tests using infrared and visible light sources, measurements with soft X-ray photons and a beam of high-energy charged particles. The main parameters of the MIMOSA chips, determining the feasibility of the novel technique for silicon position sensitive detectors, were evaluated. The emphasis was put on tests aiming at estimation of the collected charge, properties of charge collection mechanism, SNR, spatial resolution and detection efficiency. The tests with a high-energy particle beam performed at the CERN particle accelerators were preceded by laboratory measurements of more elementary quantities. The laboratory tests included examination of the signal dynamic range, time response of the device to the light pulses, efficiency of the pixel reset operation and charge-to-voltage conversion gain. Temporal noise and spatial non-uniformities in pixel responses, including fixed pattern noise evaluated for a whole array of pixels, pixel-to-pixel variation of the conversion gain and properties of the lateral charge spreading onto the neighbouring pixels, were also studied. Two methods were used to cross check, i.e. exploiting soft X-rays and Poisson statistics of shot noise. Measurements with a pulsed power infrared laser source allowed evaluating the charge collection time. The first estimation of radiation hardness limits for the MIMOSA chips were determined in irradiations with protons, neutrons and X-ray photons. Immunity to different kinds of radiation, not only excellent tracking parameters can be decisive for the possible use of this detection technique in future high energy physics experiments. The test programme has been complemented by studies of influence of the strong magnetic field on electrical operation of the devices and their detection performance.

6.2 Experimental Set-up and Procedure

6.2.1 Read-out of MIMOSA

All tests of the MIMOSA chips were performed with a specific data acquisition system based on the VME bus protocol. The simplified schematic diagram of the experimental set-up for MAPS detectors characterisation is shown in Figure 6-1. The environment for control, data acquisition and signal processing was built around the ELTEC E-16 processor running OS/9 and the 8 and 12 bit versions of the precision general purpose VME Flash ADC Unit for the Strip Detector Readout (VFAS) modules [96] installed in the VME crate. The bare MIMOSA chips were wire-bonded onto the small PCB card called the *Front-End Board*. The Front-End Board comprised the first stage external amplifiers buffering the signals from the chip and tuneable sources of bias currents needed for detector operation. The Front-End Board was connected by a flexible ribbon cable to the second card. The latter was called the *Interface Board*. The Interface Board was an interface stage between the chip under test and the VME processor. It was used for two directional transmissions of digital control signals between the chip under examination and the VFAS card and for transmission of the analogue data for digitisation. The set of low noise amplifiers, converting single-ended analogue outputs of the *Front-End Board* to differential transmission lines connected to the ADCs inputs, was mounted on the interface card. The analogue information from the pixel device under test was digitised by one 12 bit precision VFAS card. The 12 bit resolution VFAS card features two independent ADC channels with maximum conversion rate of 40 Msamp/s, and it was possible to process simultaneously data from arrays of pixels. Two optional, 8 bit precision VFAS cards featuring four independent ADC channels were installed in the system depending on the tests purpose. During the tests with high-energy particle beams, the part of the data acquisition system with the VME processor needs often and unlimited access by the operator. In order to obey security regulations, it cannot be placed together with the tested detector exposed to the beam in the beam zone. Thus, the analogue amplifiers on the Interface Board were designed to drive up to 30 m long cables, connecting the detector to the data acquisition system. The Interface Board is also used for generation and distribution of the analogue and digital power supply voltages and for generation of proper reference voltages for the on-chip and external amplifiers. The generation of power

supplies includes voltages supplying the MIMOSA chips tuned to +5 V, +3.3 V and +2.5 V as a function of a chip version under test, ±6 V for analogue amplifiers and +5 V for digital circuits. The full digital control was handled by a XILINX FPGA* chip based, programmable logic unit installed on the VFAS card. It included frame and line synchronisation, timing verification, and generation of the test patterns.

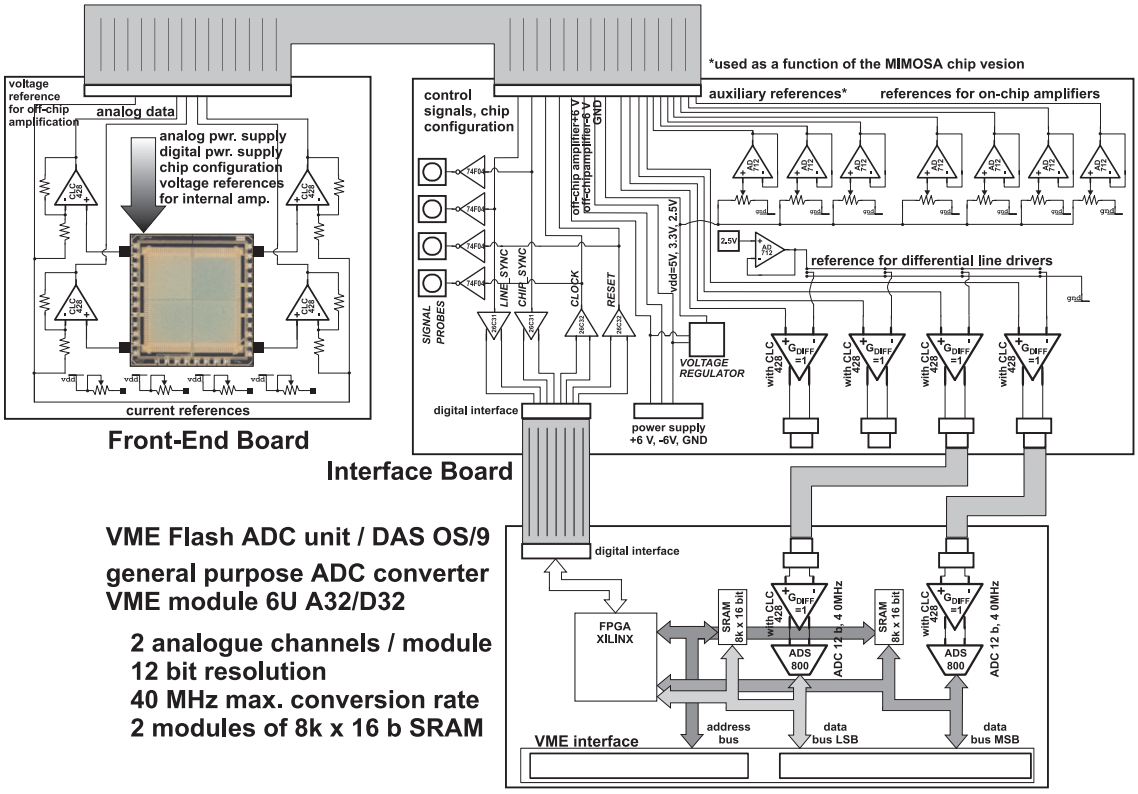

Figure 6-1: Experimental set-up for MAPS detectors characterisation.

The digital test patterns, provided by the VFAS module were limited to two signals only, needed to drive the MIMOSA chips i.e. the read-out clock and the reset signals. These signals were transmitted via the digital I/O port. Some lines of the port were configured as inputs, and received synchronisation signals sent by the chip under test and the read-out clock signal looped back from the Interface Board. The return clock could be used for analogue-to-digital conversion, allowing better synchronisation with the analogue data for the same lengths of the analogue and digital cables regardless the delay.

The individual pixels in the array of the chip tested were addressed in consecutive clock

* FPGA stands for Field Programmable Gate Array.

cycles and the samples, digitised with 12-bit resolution, were stored in the local on-card SRAM* memory. For the VFAS card used, the acquisition rate per channel could be chosen from one of the predefined frequencies i.e. 0.625, 1.25, 2.5, 5 and 10 MHz. The Mimosa I chip was tested at the three lower speeds of read-out clock, and remaining chips, whose output buffers were designed fast enough for the 10 MHz data throughput, were tested at the highest read-out frequencies as well.

During all tests, the pixel sensor was kept at constant temperature. These test conditions were reached using a mixture of water and ethanol circulating in the dedicated cooling system or by putting the device into a refrigerator. The major motivation for cooling was to achieve more convenient test conditions by increasing the time interval between consecutive reset cycles. The cooling reduced the leakage current and the reset cycle could be slowed down to a few Hz. The diode leakage current modifies the voltage of the charge-collecting node. If the leakage current is too high, this voltage, amplified on the chip, moves rapidly out of the dynamic range of the ADC. In order to verify the detector performance, all the tests were also repeated at room temperature. No significant degradation was observed with increasing temperature, including SNR and tracking parameters. It was verified during the tests that the device cooling has a negligible effect on the measured noise. The cooling does not affect the noise performance, since the contribution of the shot noise due to the leakage current is negligible for practical frame rates compared to other noise sources. The cooling was important for convenience of the beam tests, where the triggers were randomly distributed in time and the spill time were not synchronised with the pixel resetting. Most of the measurements, especially the beam tests of the MIMOSA I chip, were done at a temperature below 0°C i.e. between –10°C and –20°C. In the case of the remaining chips, most of the measurements were performed at room temperature. Convenient room temperature operation was possible for the MIMOSA II, III and IV, since a higher read-out frequency was used and the diode reverse current was an order of magnitude lower due to the different fabrication process used for these devices.

Basic prototype parameters, such as the total charge-to-voltage gain and the pixel equivalent noise charge, were determined with a 5.9 keV X-ray source of ^{55}Fe and a source of visible light. The charge collection time was measured with infrared laser shots. The chips

* SRAM stands for Static Random Access Memory.

were tested with pion beams of 15 GeV/c and 120 GeV/c from the CERN PS and SPS* accelerators, respectively.

6.2.2 Set-up for X-ray Source and High Energy Particle Beam Tests

The MIMOSA chips were extensively tested with ionising radiation. All chips were exposed to soft X-rays from a radioactive source, while the tracking performance of high energy charged particles was evaluated only for the MIMOSA I, II and IV chips.

The local memory, in which the digitised 12 bit resolution samples were stored, was organised as a circular buffer memory. Following a reset pulse, the MIMOSA output was constantly sampled at the read-out frequency, and the data digitised were written continuously to the memory waiting for a trigger signal. The memory depth on the VFAS card used for testing the MIMOSA I and II chips was 8192 of 16 bit samples, allowing storing two consecutive 64 × 64 pixel images from the detector. Later versions of MIMOSA were tested with a new generation of the 12-bit resolution VFAS board, which was equipped with four independent ADC channels with 512 k × 16b of SRAM assigned to each channel and a XILINX chip which can be programmed to realise algorithms for on-line data processing [97]. The circular architecture of the memory for one read-out channel, identified with a single array of pixels from the tested chip, is shown in Figure 6-2.

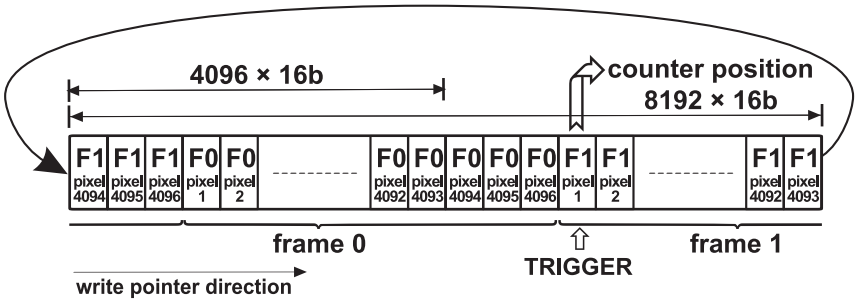

Figure 6-2: Circular architecture of the memory for one read-out channel.

In the first version of the VFAS card, information from two consecutive frames was kept in the memory. The data acquisition principle was based on the correlation in terms of the reset cycle of both frames in the memory. The data validation was given by an external triggering signal. When the incoming trigger coincided with the gating signal indicating the

* CERN PS and SPS stands for Proton Synchrotron and Super Proton Synchrotron accelerators located at CERN.

readiness of the system for new data, the data acquisition was stopped with the delay corresponding to the read-out time of one frame. Then the memory contents was transferred by the processor to the hard disk guaranteeing the particle signal to be present in the image resulting from subtracting two stored frames. The gating signal was activated, when the read-out of the first frame, defining the first reference, was finished. This procedure was applicable depending on the trigger availability, which could be due to the detected particle in the plastic scintillator in the case of the beam tests. Thanks to this read-out method, an image of the entire array with its state before and after the particle arrival was available for the analysis. This approach, which takes advantage of the trigger is obviously only possible in the case of the beam tests. During the tests with X-ray photons, where no trigger was available, the signal emulating a continuous trigger was delivered and the data were transferred to the disk immediately after the second frame became available in the memory. The fact of having two consecutive images available in the memory allowed performing the correlated double sampling (CDS) signal processing. One special memory register was used to store a pointer called *Counter Position* to indicate bounds of both acquired frames and to reconstruct proper synchronisation in terms of the frame arrival time. Figure 6-3 presents, in a strip-like display format, an example of the two consecutive frames raw signal samples acquired at –20 °C by the array of single-diode pixels in MIMOSA I. The corresponding result of the CDS processing is shown on the right-most plot. A few points sticking out the background in the Figure 6-3c represents pixels touched by particles.

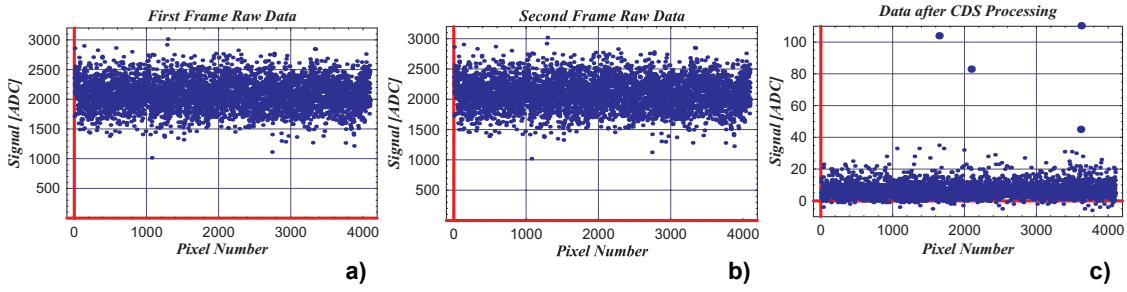

Figure 6-3: Example of the raw data for the single-diode pixel configuration in MIMOSA I, (a) first frame, (b) second frame, (c) remainder after two frames subtraction – equivalent to the CDS processing.

The remaining signal after CDS represents the charge due to leakage currents in each pixel. The distribution is centred on a non-zero mean value. It is non-symmetric, which results

from the presence of pixels exhibiting increased leakage currents.

The response of the MIMOSA chips to soft X-ray photons was examined with the source of the relatively high activity ~20 mCi mounted in front of the detector under test in the way allowing having single hit per frame in average. Typically used read-out clock frequencies were set to 1.25 MHz, 2.5 MHz, 5 MHz and 10 MHz (except for MIMOSA I), resulting in a frame acquisition times of 3.27 ms, 1.63 ms, 0.82 ms, and 0.41 ms for MIMOSA I, II, and IV, respectively. For MIMOSA III the frame rates were adequately four times longer. Limited number of hits per single read-out frame allows conveniently to avoid any unwanted bias in the data analysis and also easier verification of data analysis algorithms. Limiting the number of hits is also very useful for monitoring the detector operation during data acquisition. Any abnormal state, seen as artefacts and patterns on the acquired images, could be effortless identified and debugged being easily distinguished from correct signals.

The response of the MIMOSA chips to MIPs traversing a CMOS sensor was studied using high-energy particle beams at CERN. For these tests, pixel detectors were mounted inside a high precision beam reference telescope [98]. The beam telescope is based on eight individual planes of high precision silicon microstrip detectors to measure the trajectories of the impinging particles. Each detector has a size of (length × width × thickness) equal to 12.8 mm × 12.8 mm × 300 μm. The conceptual diagram of the test set-up with the silicon beam telescope and the MIMOSA detector under test is shown in Figure 6-4.

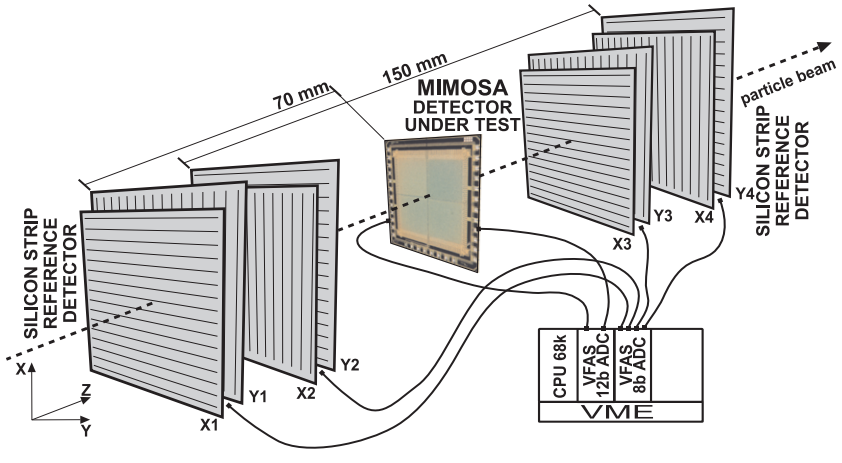

Figure 6-4: Test set-up with the silicon beam telescope and the MIMOSA detector under test for the beam tests.

The reference detectors were arranged in four individual pairs measuring particle

positions in two orthogonal co-ordinates X-Y. Two detector pairs were installed upstream and two downstream the sensor under test. The distance between upstream and downstream modules were about 150 mm. A total of 256 strips per plane were read out with low noise VA2 electronics [99]. The strips in the module were oriented in the order of XYYX. The analogue information from the modules of the silicon beam reference telescope was digitised by the additional 8-bit resolution VFAS card installed in the system. Two scintillation counters in coincidence, not shown in Figure 6-4, provided a fast trigger for the data acquisition system. Two scintillator pairs were used: the scintillators had an active area of 2×2 mm^2 and 7×7 mm^2 in the first and second pair, respectively. The scintillating counters were mechanically aligned with the sensitive are of a chosen array of pixels in the MIMOSA chip under test. For handling the trigger signal and synchronisation of the MIMOSA chip with a high resolution telescope two additional lines, apart of that used for test pattern generation and control signals reception, of the I/O port on the VFAS card were configured. The typical trigger rate during each spill (600 ms for PS and 5.1 s for SPS) was within the range from a few hundred Hz to 1 kHz, but only a fraction of triggers up to a few tens per spill could be accepted by the acquisition system based on the slow VME OS/9 processor.

The acquired raw data were recorded on EXABYTE tape or on the hard disk of the PC computer under LINUX connected to the OS/9 processor in the VME crate by an ETHERNET link. The data files recorded in a custom defined binary format were typically 2000 events long. Longer test runs were split into multiple files. Each file contained data from two separate ADC channels of the VFAS card. Events were 32768 byte long and data were grouped into 64 bit long packets corresponding to pixel signals from both channels. Although the signals were digitised with 12-bit precision the results were stored in 16 bit long words. The first 16 bits of each packet corresponded to the second ADC input and the acquisition time after trigger arrival (conventional in the case of the X-ray tests), the next 16 bits contained information from the first ADC input for the same pixel number and the acquisition time, the following 32 bits held signals from the precedent frame for the second and the first ADC input, respectively. Only the first 50 events, up to filling up the memory on the VME processor, were acquired at the maximum speed of 3.5 event/s. Then, the content of the buffer memory was consecutively transferred to the disk through the ETHERNET connection and the new data were acquired as memory locations were freed. The

ETHERNET connection and writing data to the disk were the rate limiting elements during the data acquisition. Each data acquisition was followed by a single reset cycle, and the new data could be acquired immediately after the trigger signal could be internally accepted.

The recorded data were off-line analysed using ROOT or Mathematica based programs. Simplified on-line monitoring was implemented in the processor used for the data acquisition and stand alone programs based on LabVIEW and Mathematica were also used in order to get a fast and relatively precise estimation of the prototype performances i.e. noise, hit rate, signal amplitude, etc. during the tests.

6.2.3 Set-up for Infra-red Laser Tests

Tests with a fast-pulsed power infrared laser were carried out at CERN. The laser source was characterised by the following parameters: wavelength=1060 nm, rise time=0.2 ns, pulse width=8.5 ns, spot size=10 μm (FWHM). Infrared light of the wavelength within the range used in the experiment is able to fully penetrate silicon detectors, and their response to the light pulses resembles MIPs. The test purpose was to measure the time properties of the pixel response. The laser power was tuned to simulate the amount of charge created by a single MIP in the single light shot. The special set-up, which was used during these tests, is shown in Figure 6-5. It consists of an X-Y table with the laser source with optics attached to the mobile arm and connected to two laser drivers by means of a fibre link. Two laser drivers were available, the first one of 660 nm wavelength for a coarse and fast laser positioning, and the second one of 1060 nm for testing the pixel response. The position of the laser beam over the selected pixel was fixed on the X-Y table maximising the signal amplitude for a given pixel. During each measurement only one pixel was selected for readout. The VFAS card was used for generation of the reset pulse and addressing a selected pixel for read-out. The address of the pixel was determined by the number of read-out clock cycles counted from the beginning of the reset operation. The laser pulse was triggered by a fast 50 MHz pulse generator, and the typical delay of the laser driver on the trigger signal was about 65 ns. The analogue response of the pixel was recorded as a function of time using a fast digital oscilloscope connected via a GPIB link to a PC computer. The ASCII data were downloaded onto the computer hard disk under control of a simple LabVIEV program.

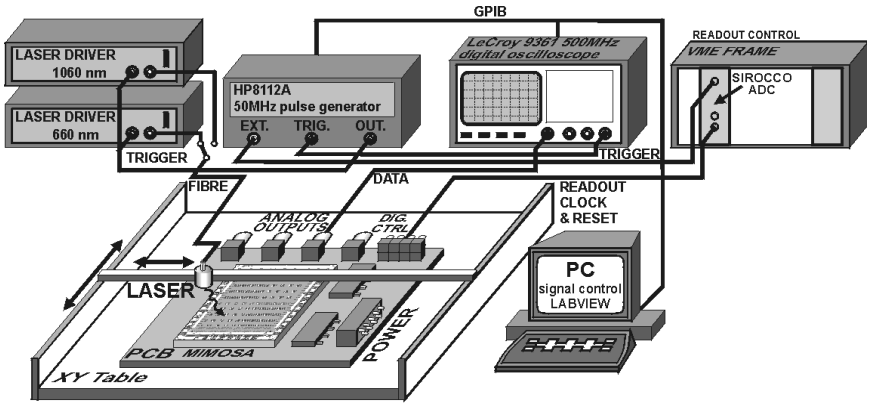

Figure 6-5: Set-up used for tests with infrared laser.

6.3 Signal Dynamic Range

Signal dynamic range is also referred to as full well capacity. This quantity addresses the maximum charge collected on the charge-sensing node, which can be handled in the read-out. The correct read-out operation requires all transistors in the analogue part of the read-out chain operated in their active regions. Usually, full well capacity is expressed in number of collected charge carriers i.e. electrons. The main concern, when discussing signal dynamic range, is related to the current source transistor providing bias current to the pixel source follower. This transistor goes first out of the saturation region when the signal magnitude increases. These effects degrade the gain of the source follower. The current source transistor is usually designed with a small size W/L ratio. It leads to minimisation of the small-signal transconductance of the current source transistor. This design procedure results from the noise optimisation. Thus, the saturation voltage V_{DSsat} of the current source transistor is relatively high. For the typical bias currents between 10 μA and 25 μA, this voltage varies for different versions of the MIMOSA chips, and it falls within the range between 200 mV to 450 mV for MIMOSA I and III, respectively. The second factor decreases the full well capacity is the power supply voltage. The maximum allowed value of the power supply decreases with decreasing feature size of the process, while the capacitances of the charge sensing node remain almost unchanged to maximise the charge-to-voltage conversion gain. Another limitation of the full well capacity value comes from the maximum voltage level achieved after resetting of the charge sensitive node. This voltage is usually below the power supply level, because of only partial efficiency of the rest operation,

which measurement are given in Chapter 6.5. Table 6-13 gives a summary of approximate values of the full well charge capacity of different versions of the MIMOSA chips obtained in tests at nominal power supplies, bias conditions and reset operation performed after each two frames acquired. The quoted values of the charge-to-voltage conversion capacitances were obtained in measurements presented in the following chapters.

Table 6-13: Full well charge capacity of different versions of the MIMOSA chips. (*chip versions with radiation tolerant pixel layout)

	MIMOSA I 1-diode	**MIMOSA I 4-diode**	**MIMOSA II 1-diode r.t.***	**MIMOSA II 2-diode r.t.***	**MIMOSA III 1-diode r.t.* W/L=3.8/0.57**	**MIMOSA IV 1-diode r.t.***
Charge-to-voltage conversion capacitance	10.9 fF	26.6 fF	7.0 fF	9.1 fF	12.6 fF	8.6 fF
Full well charge capacity	~136 ke^-	~332 ke^-	~44 ke^-	~57 ke^-	~39 ke^-	~43 ke^-

6.4 Tests under Infrared Illumination – Time of Charge Collection

The goal of this experiment was to examine time properties of charge collection from an undepleted epitaxial layer in the case of the MAPS detectors. The time of charge collection was estimated exploiting a laser source emitting short shots of infrared light using the test set-up used for tests under infrared illumination is provided in Chapter 6.2.3. A typical measured time response to the single light pulse of a magnitude tuned to simulate MIPs is shown in Figure 6-6. The tests were carried out for the MIMOSA I chip, and this figure presents results obtained for the single diode pixel configuration. The estimated fall time of the signal is about 200 ns, but it does not characterise the actual pixel response. The latter is considerably slowed down because of slow time response of the analogue circuitry in the read-out. In order reproduce the original signal to be measured on the charge sensitive node in the pixel, the measured curve was deconvolved with the transfer function of the on-chip amplification stages.

For modelling the output amplifier and the pixel source follower, single-pole transfer functions featuring low-pass filter characteristics were assumed. Thus, the transfer function of the amplifier $H_{amp}(s)$ in the MIMOSA I chip is described by a second order low-pass

filter

$$H_{amp}(s) = \frac{A}{s+a} \cdot \frac{B}{s+b}, \tag{6-1}$$

where the coefficients $A=128.5\times10^6$, $a=139.1\times10^6$, $B=45.6\times10^6$ and $b=12.3\times10^6$ could not be measured directly and have been only estimated by SPICE-type (SPECTRE) simulations.

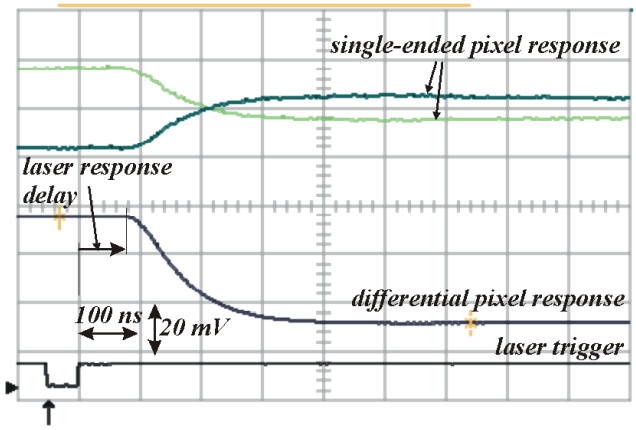

Figure 6-6: Typical pixel response for the single-diode pixel in the MIMOSA I chip to the infrared laser shot.

The Laplace transform $S(s)$ of the measured output signal $s(t)$ is a product of the transfer function of the amplifier and the transform $E(s)$ of the unknown signal $e(t)$, representing the original pixel response, which can be written down as

$$S(s) = H_{amp}(s) \cdot E(s) \Rightarrow E(s) = \frac{S(s)}{H_{amp}(s)}. \tag{6-2}$$

This original pixel signal was recovered by discrete differentiation of the measured response according to the following differential equation

$$e(t) = \frac{1}{A \cdot B}\left[\frac{d^2 s(t)}{dt^2} + (a+b)\frac{ds(t)}{dt} + a \cdot b \cdot s(t)\right]. \tag{6-3}$$

According to this simple method, the time of the charge collection for the infrared laser signals was found between 50 ns and 70 ns for both pixel configurations in MIMOSA I, i.e. the single-diode and four-diode pixel configurations. These values are considered slightly optimistic because some undershoot (about 2% - 3%) is observed on the deconvolved signals, as is shown in Figure 6-7. The presence of the undershoot suggests that the actual time response of the filter is slightly faster than the one estimated in SPECTRE and used for

deconvolution. Better reproduction, without any undershoot, is achieved varying the parameters of the filter. After some adjustment the real charge collection time is estimated to be rather close to 100 ns and 60 ns in the case of the single and four diode pixel configurations in the MIMOSA I chip.

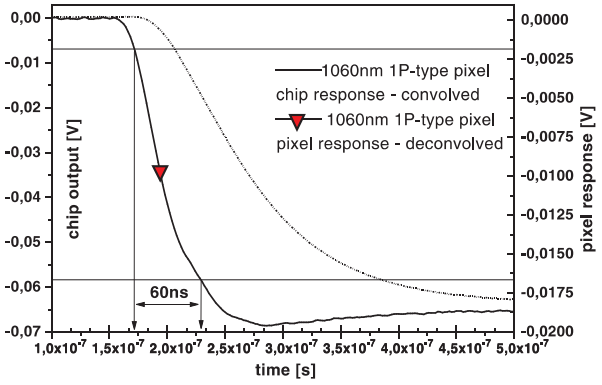

Figure 6-7: Example result of deconvolution of the pixel response for the single-diode pixel in the MIMOSA I chip.

Since the laser power sets the ionisation rate close to that from high-energy particles and the beam was well focused, the second outcome of performed tests with infrared illumination was the first estimation of the expected cluster size from minimum ionising particles. The laser position was fixed on one pixel. First, the central pixel and then its nearest neighbours were addressed to be read out. The magnitude of sensed signal was a monotonically decaying function of the increasing distance from the central pixel. The fourth pixel in the course of decreasing signal magnitudes, chosen from a range of pixels constituting a cluster of closest neighbours, featured a signal of on average less than 10% of that detected on the central pixel.

The experiment with infrared illumination confirmed the results of the device simulations presented in Chapter 4, and prior expectations on the limited charge spread and the relatively fast charge collection of the designed devices. The results indicated the time of charge collection in the range of about 100 ns and a charge spread to a few pixels adjacent to the central one.

6.5 Efficiency of Pixel Reset Operation

Efficiency of the pixel resetting operation was tested applying the reset signal to the

MIMOSA chip and stopping read-out clock after a few first cycles. Thus, evaluation of the voltage on the charge-collecting node during reset operation was observed on a dummy pixel. The dummy pixel in the MIMOSA I chip is a fully functional cell and is identical to that used in the array. It is used to prevent the voltage on the common read-out line from dropping to zero during the reset phase. For this time, all row-selecting switches in the array of pixels are in their state off and there is no source follower transistor in the array conveying the current. If the read-out line voltage dropped to zero, it would need some time to rise up at the beginning of the read-out phase. This time could be more than several read-out clock cycles, thus several pixels from the beginning of the first frame risk being lost at the transition from the reset and read-out phases. The dummy pixel is connected to the readout line during the reset phase. Additionally, its reset transistor is activated for the whole reset phase making possible examination of the reset voltage evaluation.

Figure 6-8 shows oscillograms of the dummy pixel output voltage increase during the reset phase under strong illumination with visible light and in the dark performed at different temperatures –12°C, 0°C and 28°C. Visible light illumination was used to simulate increased leakage current of the charge collecting diodes, which results in a faster achievement of the steady state.

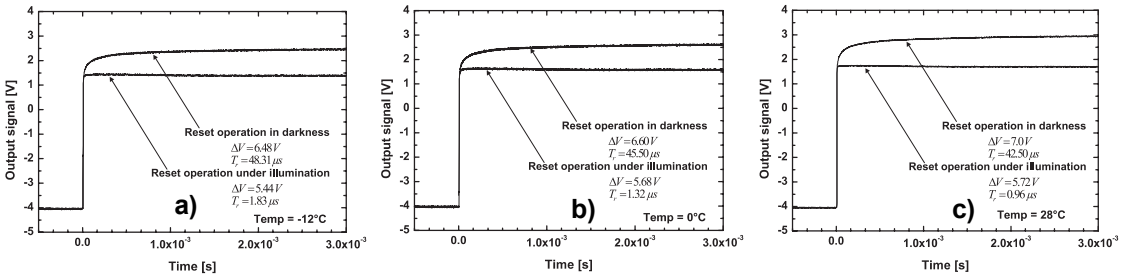

Figure 6-8: Illustration of pixel reset operation under strong illumination and in obscurity performed at different temperatures (a) –12°C, (b) 0°C and (c) 28°C.

The results obtained experimentally fully confirm prior analytical considerations on the time properties of the reset operation, which were presented in Chapter 5.5. In the darkness, the increase of the voltage on the charge collecting node is slow and several hundred milliseconds is required to achieve the steady state conditions. Since steady state is not reached, the final reset voltage can depend on the diode voltage at the beginning of reset. In practical applications, where the reset intervals are short the reset is incomplete. For visible

light application the dependence of the reset voltage on the state at the beginning of the reset operation results in image lag. Under strong illumination, in contrast to the operation of the detector in darkness, the increase of the reset voltage is fast, and the steady state is achieved within first microsecond after applying the reset signal. The influence of temperature on the reset operation is twofold: firstly, the temperature affects reset speed in absence of any external excitation source via the temperature dependence of the diode leakage current, and secondly, it modifies the pixel output voltage level because of the temperature dependence of the threshold voltage of the source follower and reset transistors.

Overdriving the reset transistor gate can eliminate incomplete reset. This goal can be achieved either by biasing the reset transistor drain at a voltage lower than the gate potential during the reset phase or by the use of a bootstrapping reset circuitry [100]. The latter approach is based on the voltage pumping principle in the switched capacitance circuit and increases the complexity of the pixel design by adding new transistors and it cannot be done without the use of PMOS devices. On contrary, biasing the drain of the reset transistor at the voltage lower than digital power supply, allows to overdrive the reset transistor, which for the whole reset phase operates in the linear region. Thus the final reset voltage is independent of the initial diode voltage, and there is no need to use PMOS devices.

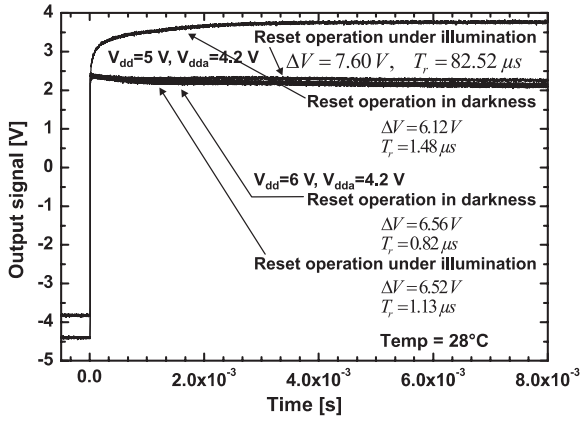

Figure 6-9: Illustration of pixel reset operation under strong illumination and in the dark performed at the temperature 28°C for different analogue and digital bias conditions.

Figure 6-9 shows the pixel resetting operation at a temperature of 28°C under strong illumination and in obscurity for reduced bias of the reset transistor drain at 4.2 V and two

values of digital power supply, i.e. 5 V and 6 V. The fast and complete reset is achieved for the drain bias node potentials of the reset transistor satisfying the condition $V_{DG} > V_{TH}$.

The effect of incomplete reset is strongly manifested in the data acquired during the test with high-energy particles. Figure 6-10a shows example of data taken during the tests at CERN SPS on the 120 GeV/c. Each point in the plot represents average value of the measured signals calculated over the total number of pixels in the array. The spill interval and the cycle interval were 5.1 s and 16.8 s, respectively. The MIMOSA I detector was operated continuously, but the reset operation was performed only after each accepted event. In the cases, where the time to wait for a trigger signal was long, the voltage on the capacitance of the charge sensitive node was significantly decreased. The constant leakage current was discharging the conversion capacitance, leading to significant variations of the initial voltage for each reset phase. In contrast to long idle periods, the average level of the reset voltage during periods of high trigger density, i.e. the spill time, was being continuously increased. The increase of the average level was due to the increased repetition of the reset operation. Fortunately, the variation of the average level does not introduce any temporal fluctuations during the read-out phase following the reset operation. The fluctuations in the measured signals can be eliminated using CDS processing as it is shown in Figure 6-10b. The periodic spill pattern is fully eliminated. Special care is needed to provide signal swing large enough for the raw data to cover the whole range ensued by fluctuations of the average level due to the incomplete reset operation. This requirement is important in a system exploiting MAPS detectors, where the raw data are transmitted and the data processing, including CDS, is done externally to the detector.

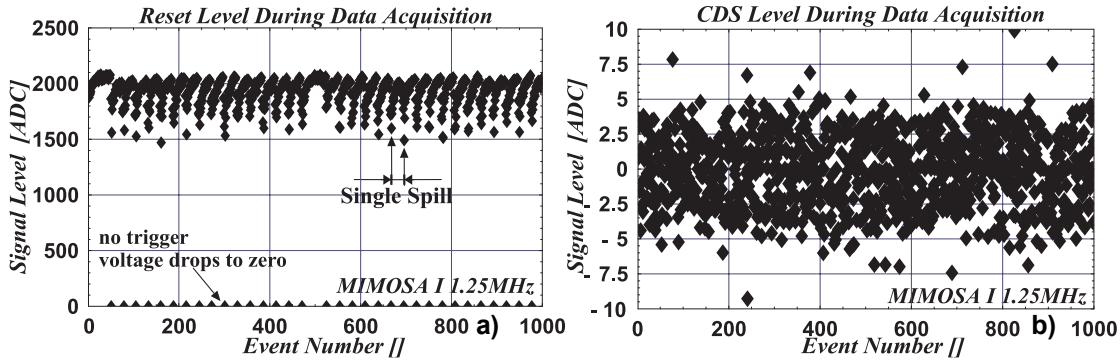

Figure 6-10: Effect of partial pixel reset for triggered data acquisition for signals (a) before and (b) after CDS.

6.6 Tests with Soft X-rays and Noise Performance

Extensive tests with soft X-rays from a radioactive ^{55}Fe source have been carried out prior to the exposure of the MAPS detector prototypes to a high-energy charged particle beam. Low energy photons were chosen because of their efficient absorption in silicon and the amount of the generated charge close to that expected as available for collection from the epitaxial layer for MIPs.

6.6.1 Signal Extraction and Data Processing

The data analysis started with separation of the data from two ADC input channels and calculation of the result signal in a single channel as a difference between the signal amplitudes in two consecutive frames. This subtraction corresponds to the CDS processing. As a result of the subtraction operation on the data taken from the binary files, new files written in the ASCII format were created. The signal remaining after the first processing is a combination of signals referred to as constant in time pedestals resulting from integrated leakage current, sporadic photon interactions considered as a sought signal, and noise contributions from thermally generated leakage current and signal fluctuations in the read-out electronics. Figure 6-11 shows an example of the raw data, as they are stored in the binary file, acquired for the single diode pixel configuration of the MIMOSA I chip. As it is shown later, some signals due to photons are present in the data from this figure, but on this stage of the analysis it is almost impossible to correctly identify hits.

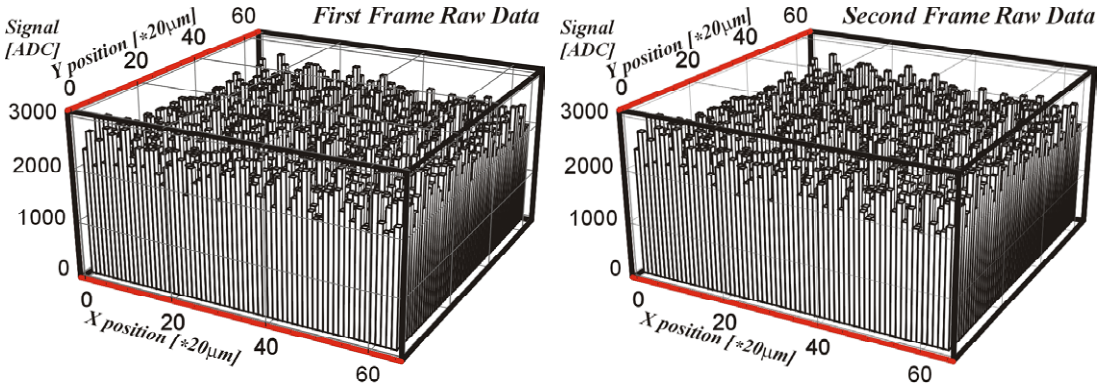

Figure 6-11: Example of the raw data of two consecutive frames before subtraction.

Raw data suffer from high frame-to-frame base line variations, single frame pixel-to-pixel

non-uniformities and increased temporal noise levels.

Figure 6-12 presents the remainder after two frames subtraction, where the raw data from the previous figure were used. The average signal level dropped dramatically, and some regions of the image could already be identified as containing potentially useful signals.

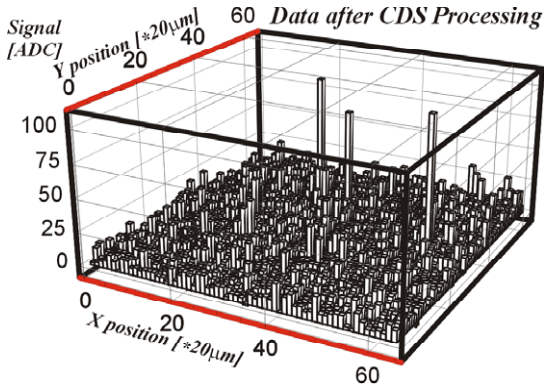

Figure 6-12: Example image after CDS processing.

The signal $s_n(k)$, after CDS processing on the pixel numbered k and in the n^{th} acquired event, called also *image*, can be expressed in terms of the expected physical signal due to the interaction $s_n^e(k)$, the random signal variation $s_n^r(k)$, the pedestal $s_n^p(k)$, and the common mode shift $s_n^c(k)$ by the equation

$$s_n(k) = s_n^e(k) + s_n^r(k) + s_n^p(k) + s_n^c(k). \tag{6-4}$$

These quantities, through all the analysis, are measured in the ADC units and can be identified with equivalent charges integrated on the diodes within each pixel. The sought quantity $s_n^e(k)$ is the physical signal due to the interaction in the detector and is to be distinguished from the noise $s_n^r(k)$, which occurs randomly. The pedestal $s_n^p(k)$, assuming the acquired data were taken in the absence of any excitation source, is calculated by

$$s_n^p(k) = \frac{1}{N}\sum_{n=1}^{N}\left[s_n(k)\Big|_{\text{no signals}} \right] = \frac{1}{N}\sum_{n=1}^{N}\left[s_n^r(k) + s_n^p(k) + s_n^c(k) \right], \tag{6-5}$$

where N is a number of acquired images. In practice, when the physical signals are present in data, it is not obvious how to estimate pedestals. The simplest pedestal estimator can be calculated averaging measured signals over N events without suppressing physical signals.

The pedestal estimator using this approach is given by:

$$s_n^{p\,est}(k) = \frac{1}{N}\sum_{n=1}^{N}\left[s_n(k)\right]. \tag{6-6}$$

It is apparent that, the pedestal estimator expressed in equation (6-6) is biased by events with physical signals. In order to evaluate the dependence of the estimator on the number of registered events with hits, and therefore on its error, two parts in equation (6-6) can be isolated. The pedestal estimator (6-6) can be rewritten in terms of a true pedestal and a contribution from hits. For a given pixel index i and assuming total number N of acquired images containing N_e events with the expected physical signals, the transformed equation (6-6) can be written as

$$s_n^{p\,est}(i) = \frac{1}{N}\sum_{n=1}^{N}\left[s_n^r(i) + s_n^p(i) + s_n^c(i)\right] + \frac{1}{N}\sum_{n:\text{hits present}}\left[s_n^e(i)\right]. \tag{6-7}$$

After some rearrangements, it can be shown that the relative error of the pedestal estimator is proportional to the product of the ratio N_e/N and the mean physical signal detected

$$\frac{s_n^p(i) - s_n^{p\,est}(i)}{s_n^p(i)} = \frac{N_e}{N}\frac{\left\langle s_n^e(i)\right\rangle}{s_n^p(i)} \quad \text{where} \quad \left\langle s_n^e(i)\right\rangle = \frac{1}{N_e}\sum_{n:\text{hits present}}\left[s_n^e(i)\right] \tag{6-8}$$

Referring to results discussed later in detail, the mean pixel signal for the tests with X-ray photons and under beam test conditions ranges between 16 ADC and 30 ADC units. The last estimation was done taking average signal measured on a cluster of pixels for the single diode pixel configuration in MIMOSA I chip and for the test set-up configuration with a particular gain of the read-out channel. The gain was given by amplifiers installed on the Front End Board, and was adjustable. The rule assumed for determining the gain during tests was the analogue signal matching the input range of ADCs in the whole range of observed pixel-to-pixel signal fluctuations. The average spread of the physical signal charge was supposed to be limited to a few pixels only with each hit entailing a cluster of nine neighbouring pixels. The chip was operated at different temperatures within the range from – 20 °C to 30 °C, for which the mean pedestal values were estimated. In order to obtain the mean value of the true pedestal estimator, the data taken without exposure to any excitation source were used. The calculations carried out on empty data resulted in the pedestal level of 0.5 and 10 ADC units, correspondingly for the lowest and highest

temperature and for the read-out clock frequency of 1.25 MHz. Thus, for an average rate of one hit per frame of 4096 pixels, the relative error for the pedestal estimator using the method expressed by formula (6-6) extends from 0.3% for the combination of the lowest signal measured at the increased temperature, to 13% for the highest signal and low temperature operation, correspondingly. It is apparent, that the high error eliminates the simplest method given by equation (6-6) from practical use. The goal is to find a pedestal estimator, which is as close as possible to the true pedestal. The simplest solution consists in taking some amount of data without an excitation source and to perform computation of the pedestal value using these empty data. Unfortunately, this approach usually fails. Generally, the pedestal value calculated according to this method cannot be used for further analyses, because even slight changes in conditions, like temperature, power supply etc., during the data acquisition need using some pedestal-follower method which can operate on the given size event window and which is insensitive to the physical signals. This remark leads to the use of so called tracked mean for pedestal calculation, which makes additionally use of signal suppressed data values. In the analysis carried out for the MAPS detectors, the pedestal estimator was calculated in two stages. At the initial stage the pedestal estimator was calculated using the event window of N_w=100 images and an event buffer which was filled 20 times successively with M=5 images from the input file. Any arbitrary value for each pixel across the events, stored currently in the buffer, which was unequal to the extreme of the buffer, was considered as the physical signal suppressed data. As a result, the extreme values were supposed to contain physical signals. For the convenience of later analyses, the frame subtraction for CDS processing was reversed, which translated to the positive values of the physical signals in the image. Thus, it was sufficient to replace maximum signals with the mean values calculated upon the four events remaining in the buffer to suppress unwanted physical signals for the pedestal estimation. Nevertheless, in order to stabilise the method, the values equal either to maximum or minimum of the buffer were replaced with appropriate mean values. The method using physical signal suppressed data is more immune to the unwanted bias than the procedure expressed by the formula (6-6). At low interaction rates, physical signals can be eliminated effectively. However, the efficiency of the method drops with the increasing probability of having two physical signals in the buffer, which is proportional to the squared ratio N_e/N. This physical signal suppressed method was used

only during the initialisation phase for event window of the first 100 events. The initial estimator of noise level $\overset{est}{\sigma}_n(k)$ was determined for each pixel along the pedestal estimator. In order to avoid overestimation of noise values on pixels, which were illuminated, the same procedure for suppression of physical signals was applied for calculating the noise estimator.

The goal of the pedestal and noise estimator calculation, achieved according to the method for physical signal suppression described above, was to determine the initial values of these quantities for the next computation stage. Following the initial phase, new pedestal and noise estimators were recalculated using another algorithm for physical signal suppression. During the second phase, the computation window had the same size of N_w=100 events as in the initial phase, but the use of the event buffer was eliminated. Instead of searching for the extreme values in the event buffer, suppression of the physical signal for each pixel in a given image was achieved by restraining the signals to the boundary limit. The decision, whether the pixel signal was to be affected, was made on the basis of the results obtained in the initial phase. The current pixel signals were compared with the values of the corresponding pedestal estimators. The values exceeding the range of three times the value of the noise estimator around the value of the pedestal estimator, either in positive or negative direction, were subjected to the procedure for suppression of the physical signals. The new pixel values were obtained by truncation of the corresponding old pixel signals to the appropriate bounds of the comparison range. Thus, the variation of pixel values in the sequence of the acquired images was confined between the upper and lower truncation limit. Similarly to the initial phase, good stability of the method was achieved. New values for the pedestal and noise estimators were computed from the suppressed physical signal data. The analysis was limited to the first N_w=100 events, i.e. one window of events, which were recognised as good events prior to the use of physical signal suppression procedure. Faulty, encountered sporadically events were excluded from the analysis. An event was recognized as faulty if a significant number of pixel signals, which was improbable to be caused by the presence of the physical signals, exceeded three times the value of the noise estimator from the pedestal estimator in one event. The limit on a number of pixels, excluding a particular event from analyses, was set to the experimentally selected value of 25% of a total number of pixels in the case of the MIMOSA chips tested. The cause of the presence of faulty events in the acquired data was not possible to be fully identified because of their sporadic

occurrence. It was interpreted as a problem resulting rather from a temporarily instable behaviour of the data acquisition system than from unpredicted state of the chip under test. It was observed that the reaction of the ADC unit to input signals, exceeding the maximum allowed level even for a short while, had consequences distorting conversions occurring some time after. Rejection of any faulty event from the window of the N_w events taken into the analysis was followed by completion of the window with the next event beyond the initial window size. The noise estimator, resulting from the initialisation, was calculated according to the standard formula for unbiased estimator of the sample variance. The two-stage initialisation was performed only once for each run. Longer runs with data stored in more than one disk file had the initialisation phase performed when the first file was accessed. Then the recursive methods for calculating the pedestal and noise estimators were used. The current values of both estimators at the end of the each file were used as starting parameters for performing the analysis on the data from the following file.

The knowledge of the pedestal and noise estimators was crucial for the next stage of the analysis in which the physical signals were being extracted. During this stage, both obtained estimators were recursively updated allowing to take into account variable conditions throughout the experiment. The procedure for recursive calculation was carried out for all events from a single run starting with the next event to the last one used for initialisation. The analysis was completed with the calculation of the common mode shift, which allowed to introduce the immunity of the noise calculation to the correlated fluctuations in the pixel signals. The common mode shift was calculated as a polynomial fit to signals from the entire image and preceded computation of new values for the pedestal and noise. In order to eliminate eventual bias of the common mode shift due to the presence of physical signals, the latter were suppressed using the pedestal and noise estimators from the preceding step. The calculation of the common mode shift for a large number of pixels is a time consuming process. Thus, only a fraction of pixels from the whole array was taken into calculation in order to speed up the analysis. The order of the fitting polynomial was chosen as a compromise between the fit accuracy and the computation time. Polynomials of first to third order were used. The best performance, quantified in the decreased mean value of the noise estimator and acceptable fast analysis, was observed for the second order polynomial fit. Only little improvement was observed using the third order polynomial. Further increase of

the order had a negligible influence on the achievable precision and was not used. The current pedestal estimator for k^{th} pixel in n^{th} event was found by using the recursive pedestal-follower-method given by

$$\left.s_n^{p\,est}(k)\right|_{n>N_w} = \frac{1}{A}\left[(A-1)\cdot s_{n-1}^{p\,est}(k) + s_n^{3\sigma\,est}(k) - s_n^{c\,est}(k)\right], \tag{6-9}$$

where $s_{n-1}^{p\,est}(k)$ is the pedestal estimator from the n-1 event, $s_n^{3\sigma\,est}(k)$ represents the physical signal suppressed value and $s_{n-1}^{c\,est}(k)$ is the estimator of the common mode shift. The weight $A = N_w/4 = 25$ was chosen experimentally to be sufficiently robust against small fluctuations and sensitive enough to follow modest time changes in the pedestals. Based on the experience gained in the preliminary analyses, a second control mechanism for pedestal computation was needed to protect against very strong fluctuations, which could escape common mode shift suppression. These were observed to happen sporadically, but the pedestal follower algorithm yielded temporarily overstated results according to formula (6-9). The influence of stepwise changed values was observed for some number of events analysed in turn. Thus, events resulting in important variations of the pedestal estimator required to be filtered out. As a result, it was ordered not to update the pedestal and noise estimators for a given event when the condition was satisfied

$$\left[\sum_{k=1}^{K_{tot}} s_n^{p\,est}(k) - \sum_{k=1}^{K_{tot}}\left[s_n^{3\sigma\,est}(k)\right]\right] \Big/ \sum_{k=1}^{K_{tot}} s_n^{p\,est}(k) > 0.33\,, \tag{6-10}$$

where K_{tot} is a total number of pixels in the tested array, and the threshold value of 0.33 was chosen experimentally. Instead of calculating new values the old pedestal and noise estimators were adopted.

An X-ray photon or a charged particle from the beam incident on the detector causes a hit in the detector plane, which should be distinct from random fluctuations. The signal charge was extracted based on equation (6-4) according to

$$s_n^{e\,est}(k) = s_n(k) - s_n^{p\,est}(k) - s_n^{c\,est}(k). \tag{6-11}$$

The hit cluster finding required a cut on the SNR threshold. The first hit was found by searching for the pixel k_s, that had the highest signal $s_n^{e\,est}(k_s)$ and whose SNR exceeded the

seed pixel signal-to-noise threshold t_s

$$s_n^{e\,est}(k_s) \Big/ \sigma_n^{est}(k) \geq t_s \,, \tag{6-12}$$

$\sigma_n^{est}(k)$ is the current single pixel noise level obtained applying the recursive noise-follower method. The pixel with the index k_s became the seed of the first hit cluster found in the array*. According to the physics, the charge collected by the seed pixel can be relatively small depending on the distance between the hit and diode positions. Thus, this cut was loose and the seed pixels were defined as pixels whose signals exceeded five times the noise level

$$s_n^{seed\,est}(k) = \left[s_n(k) - s_n^{p\,est}(k) - s_n^{e\,est}(k) \right]_{s_n(k) - s_n^{p\,est}(k) - s_n^{e\,est}(k) \geq 5\sigma_n^{est}(k)} . \tag{6-13}$$

A hit cluster contained the seed pixel and eventually contiguous neighbouring pixels. To refine the analysis, the cluster signals from adjacent pixels were taken into account. The number of neighbours depended on the array geometry resulting in eight or six closest neighbours to the seed cluster, for square and staggered array layouts, respectively. Relatively loose cut imposed on the search of the seed pixel could qualify random signal fluctuations to hits. The summed signal contributions from the contiguous pixels included into the cluster reconstruction increased the total cluster signal. Phantom hits were filtered out requiring the cluster SNR to exceed threshold cut t_n, which was more selective than the first cut for the seed pixel. The cluster noise was calculated as root mean square value of noise contributions from all pixels constituting the cluster. The usual value of the cut t_n was between 5 and 10.

The cluster finding algorithm was iterative and several clusters were allowed within one image, while the cluster around the seed pixel with the highest SNR was formed first. Then, if another seed pixel was identified, the next cluster was formed. In order not to rate twice pixels in between two distinct clusters, the closest neighbours of a previously reconstructed cluster was excluded.

In a similar way as for the pedestal estimator calculation, the single pixel noise $\sigma_n^{est}(k)$ was estimated applying the recursive follower method. The noise being the statistical error on the measurement for the k^{th} pixel in the n^{th}, was calculated from the pixel noise in the

* An alternative method, applied also in some analyses, consists in performing a sequential pass through the channels and process the value that exceeds directly the threshold.

previous event $\sigma_{n-1}^{est}(k)$ and the signal fluctuation signal in the current event

$$\sigma_n^{est}(k)\Big|_{n>N_w} = \sqrt{\frac{1}{B}\left[(B-1)\cdot\left[\sigma_{n-1}^{est}(k)\right]^2 + \left[s_n^{3\sigma,est}(k) - s_n^{p,est}(k) - s_n^{c,est}(k)\right]^2\right]}, \qquad (6\text{-}14)$$

where the value B is a weight, which was chosen as $B = N_w/4 = 25$. Although, it could be different from the weight A, the use of the same value for both weights showed very good behaviour for noise estimation as well.

Figure 6-13 shows results of pedestals and common mode shift estimation carried out for an example run with MIMOSA I chip. On the right hand side of this figure, the results obtained after pedestals subtraction and common mode shift correction are presented.

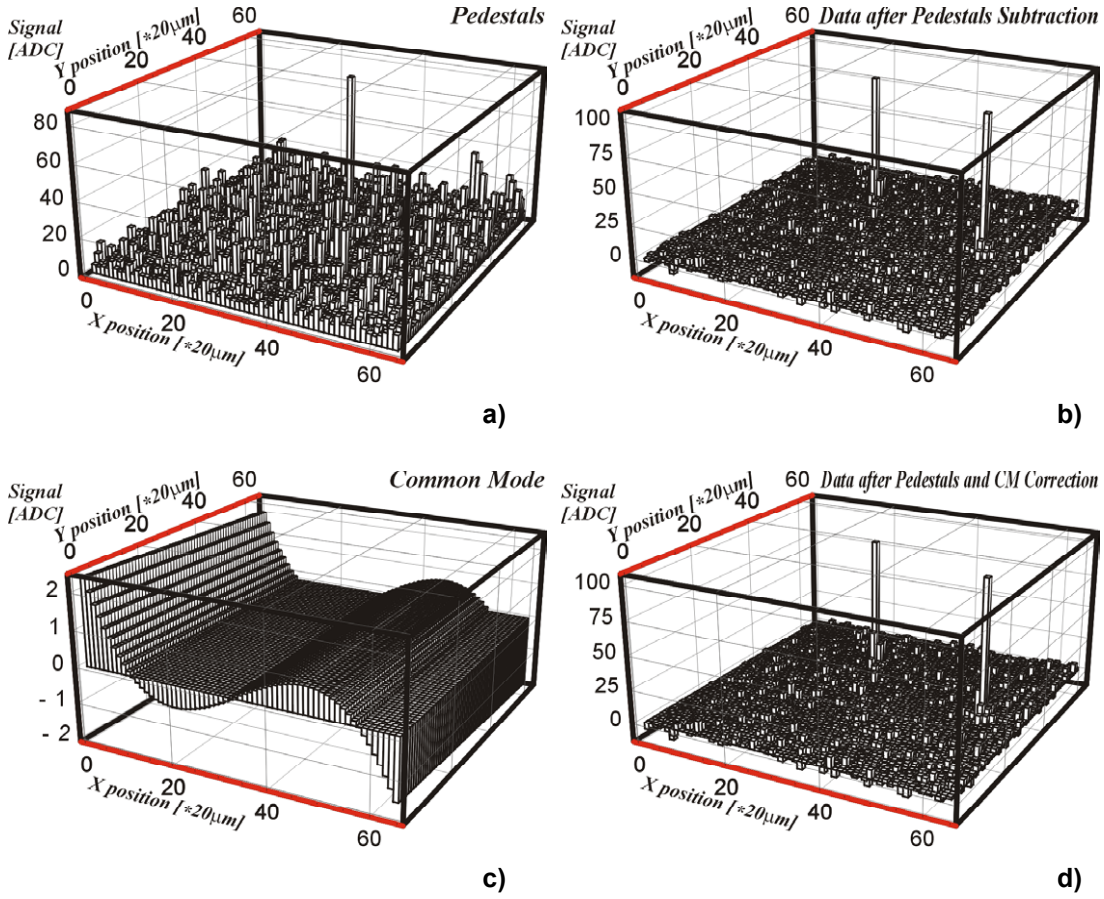

Figure 6-13: Example of data processing, (a) data from Figure 6-12 after pedestals subtraction, (b) data after pedestals subtraction, (c) common mode shift calculated for the analysed event, (d) data after pedestals and common mode shift subtraction.

The image after pedestal subtraction became nearly uniform, apart of two groups of pixels sticking out from the background. Both groups were then identified by the cluster finding algorithm, as clusters of pixels with signals due to an interaction. Non-zero pedestals, calculated for signals after CDS processing, result from leakage currents that have various origins. The main part was due to the dark current of the charge collecting diodes. Another element was the reset transistor, adding its contribution through the source-to-substrate junction and the residuary current of its off state channel. The subtraction of the common mode shift allowed correcting the data for interferences, which are, in general, of unknown origin, but exhibiting correlation for all pixels in the array. Figure 6-14a shows the spatial distribution of the temporal noise estimated by the recursive formula (6-14). The noise distribution exhibits a high degree of uniformity. The average noise level, measured as a mean value of the distribution from Figure 6-14a, varies from chip to chip. However, for all chips that were examined, only very few channels were subject to large fluctuations i.e. the temporal noise. The high level of temporal signal fluctuations might have faked real signal hits in the detector, since they could have survived the CDS processing, pedestal subtraction and common mode correction. Such fake hits vanished, once the pattern recognition came to the selection of pixels for clusters recognition on the basis of their SNRs.

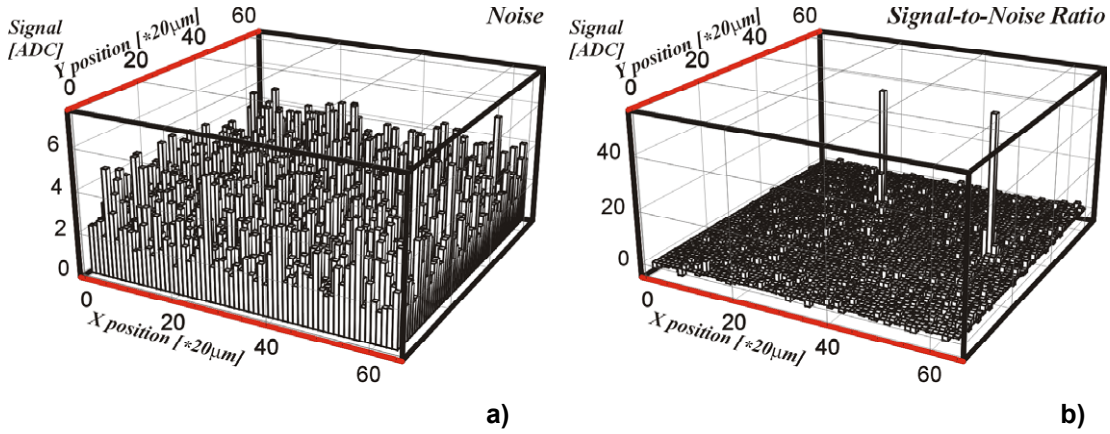

Figure 6-14: (a) Spatial distribution of temporal noise, (b) signal to noise ratio for the event shown in Figure 6-12.

The SNR distribution depicted in Figure 6-14b confirmed prior assumptions on the presence of hits in the event shown in Figure 6-12. Figure 6-15 shows two-dimensional projection of this event. Signals shown in this figure are weighted by a square root function for more perspicuous presentation.

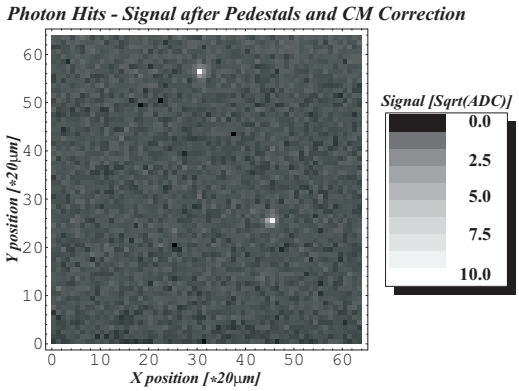

Figure 6-15: Two-dimensional projection of one event in MIMOSA I.

Figure 6-16 shows results of recursive follower method applied for calculation of the pedestal and noise estimators and the common mode shift for the single diode pixel configuration in MIMOSA I for the data acquisition run of a total length of 20×10^3 events taken during the time longer than one hour. One selected event of this run is shown in Figure 6-12. Data points in plots constituting Figure 6-16 are shown only for images in which clusters with physical signals were recognised. The chip was cooled down to –20°C by putting it into the refrigerator, and the periodic fluctuations of the pedestal mean value are attributed to the temperature variation caused by periodic switching on and off of the thermostat device.

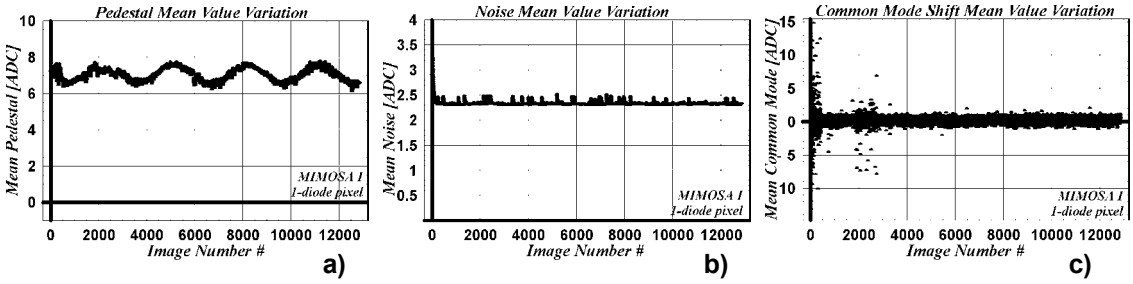

Figure 6-16: Time variation of (a) pedestal mean value, (b) noise mean value and (c) common mode shift mean value for MIMOSA I.

6.6.2 Temporal Noise and Spatial Non-uniformities

The read-out architecture of the prototype chips was realised in a very simple way without any on-line processing. This fact combined with the raw file format for the acquired data, allowed very careful and deep data analysis in terms of temporal noise and spatial non-uniformities. The data were written to the file in the form as they were appearing at the output of the ADC converter. This feature, which will probably not be available in the case

of future circuits, gave the opportunity for thorough examination and comparison of the detectors performance before and after CDS processing. Spatial and temporal noise components were evaluated in analyses carried out for different pixel configurations for chips from the MIMOSA family. It was observed, that results obtained with different configurations were leading to qualitatively similar conclusions. Thus, only results for the MIMOSA I chip are presented in a graphical form hereafter.

The first attempt to separate different noise components consisted in measurements carried out for a single pixel sampling the output repeatedly after a single reset operation. The sampling interval was 1.63 ms equal to the read-out time of one full frame, and one cycle of measurements resulted in 960 samples taken throughout 1.5648 s. In order to acquire the representative enough statistical population sample, the measurements were repeated for 1200 reset operations. Figure 6-17 shows an example of the measurement of the sampled signal variation measured on a single pixel following a single reset operation. The left hand side plot shows raw data after subtraction of the leakage current effect, causing the curve before subtraction to fall with time, and after shifting the mean value to zero. While, the right hand side plot was obtained by carrying out in turn subtractions of each two contiguous samples from the left hand plot, and then shifting to the zero mean value. The processing performed on the raw data is equivalent to CDS with the delay time constant of 1.63 ms.

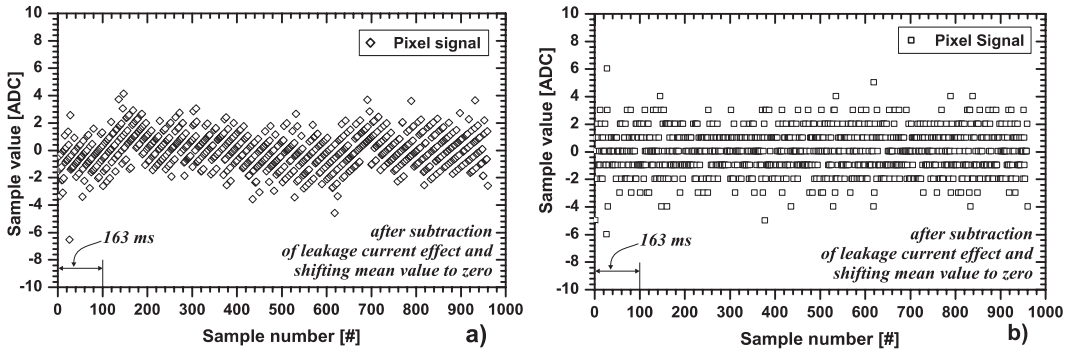

Figure 6-17: Variation of the sampled signal measured on a single pixel with a sampling interval of the read-out time of one full frame: (a) raw data, (b) after CDS.

Power density spectra of signals before and after CDS were calculated by applying the algorithm for Fast Fourier Transform (FFT). Computations were performed on sequences of samples taken after each reset operation like presented in Figure 6-17. The final spectra were obtained by averaging over 1200 data records. The resulting power spectra are given as a

function of frequency in the range limited to 306 Hz due to the long sampling interval, and are shown in Figure 6-18. The variance of temporal signal variation after each reset operation was computed by integration of the power spectra. The temporal noise level is 1.237 ADC units and 1.529 ADC units before and CDS processing, respectively. The main advantage of analysing the power spectra averaged over 1200 independent measurements was the fully efficient elimination of any irregularities present on every single spectrum. These irregularities were due to temporal disturbances in the sampled signal, and yielded power contribution at different frequencies.

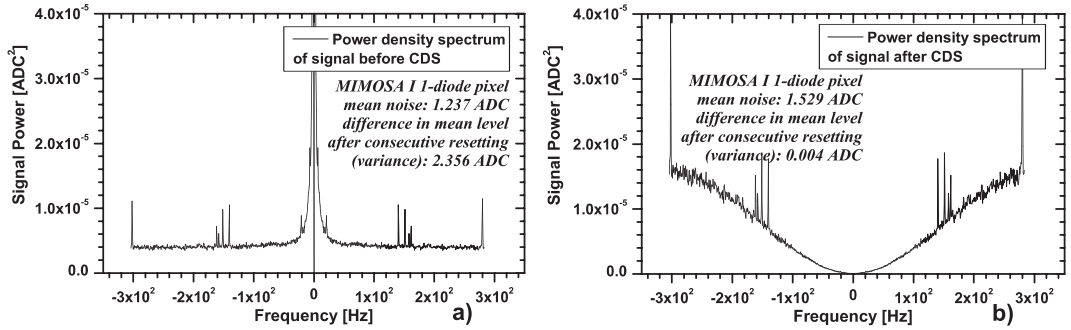

Figure 6-18: Signal power spectra [ADC²/Hz²] of (a) raw data (before CDS processing) and (b) after CDS, computed by means of an FFT algorithm on temporal samples spaced 1.63 ms.

Estimation of the kTC noise value was possible analysing variation of the mean signal calculated over the total number of the acquired samples after each reset operation. The measured variances are 2.356 ADC units and 0.004 ADC units in the case of raw data before and after the CDS processing, respectively.

Following the analyses exploiting FFT on the data taken under conditions requiring special configuration of the read-out system, temporal noise and spatial non-uniformities were evaluated for the read-out method and in the test set-up used in experiments with X-ray photons and charged particles. For both kinds of experiments, regardless the availability of the trigger signal or any other experimental condition, the data acquisition ended up with two consecutive frames stored to the disk and a reset operation was performed following acquisition of each event. The analyses presented in the remainder of this chapter address comparison of the possible physical signal extraction from the data, taking information from only one of both acquired frames, and from the data obtained in a simple subtraction of two frames. The measured noise and non-uniformities of pixel responses are particularly

important for evaluation of methods allowing to fully exploiting the potential of the MAPS devices.

Figure 6-19 shows results obtained analysing only each second frame from the acquired data, while the next figure shows corresponding results after applying the CDS processing. The first, most left plot from both figures presents a distribution of pedestals for the whole array of pixels. The variation of pedestals is significantly reduced after applying the CDS processing. The large pedestal variation before CDS results from pixel-to-pixel dispersion of the threshold voltage of the source follower transistors and only partial efficiency of the reset operation. The large dispersion of the reset voltages is due to the combination of widely spread sub-threshold parameters of the reset transistors and leakage currents in pixels. The pixel-to-pixel spread of pedestals is reduced more than 70 times after CDS. However, the distribution, formerly having a gaussian form, becomes unsymmetrical with a long tail extending towards high pedestal values.

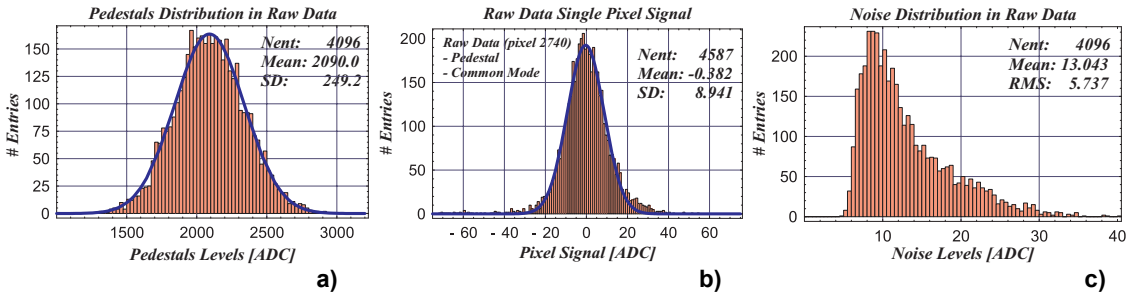

Figure 6-19: (a) Pedestals distribution calculated for raw data signals for all pixels in MIMOSA I, (b) distribution of signals on a single, chosen randomly pixel after pedestal subtraction and common mode correction calculated for raw data, (c) noise distribution in raw data.

Each entry to the histogram; shown in Figure 6-20a; is a consequence of the superposition of leakage currents present in each pixel, and is neither dependent on threshold voltages nor on the efficiency of the reset operation. The pedestal distribution after the CDS processing allows to estimate the total leakage current discharging the conversion capacitance for each pixel. The mean value of the dark current at a given temperature corresponds to the mean value of the distribution. The presence of a long tail in the histogram is related to some pixels exhibiting higher dark currents, which results from an inhomogeneous distribution of material defects. The pixels generating dark currents, which can be one hundred times higher than the average, are referred to as hot pixels [101]. Generally, a strong dispersion of the dark

current density is observed on the array.

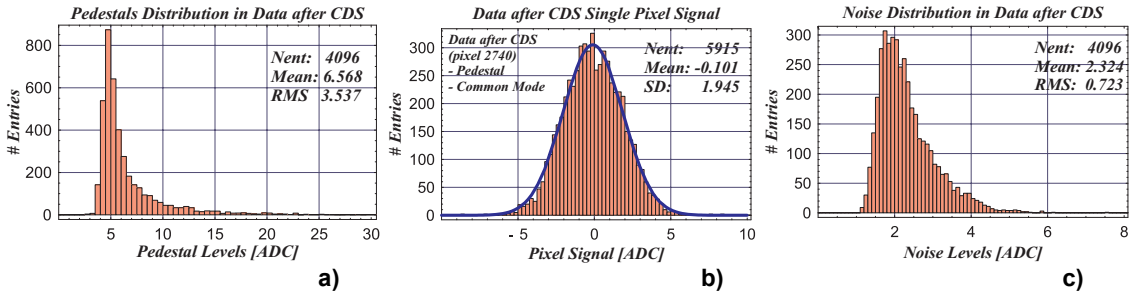

Figure 6-20: (a) Pedestals distribution calculated for data after CDS processing for all pixels in MIMOSA I, (b) distribution of signals on a single, chosen randomly pixel after pedestal and common mode correction chosen randomly pixel after pedestal subtraction and common mode correction calculated for data after CDS processing, (c) noise distribution in data after CDS processing.

The magnitude of the temporal variation of the single pixel signals calculated for data before and after CDS processing can be compared analysing plots shown in Figure 6-19b and Figure 6-20b. Both figures present distributions of the physical signal suppressed values after the pedestal subtraction and the common mode correction for a single pixel. The choice of the actual pixel for presentation from the array was made in a random way. Each entry to the histogram corresponds to different events originating from one run. The precision due to the signal digitisation is much better than the measured noise in both cases and the gaussian shape of the distribution confirms the correctness of the data analysis. The measured signal variation on the data before CDS processing is more than four times higher than for the same data subjected to the processing.

The right hand side plots in both figures present distributions of noise values calculated for the whole array of pixels. The average noise levels are 13.043 ADC units and 2.324 ADC units, before and after the CDS processing, respectively. The noise is significantly higher in the first case. One important contribution increasing the noise is due to the presence of the kTC noise. However, it is apparent that the main component increasing the noise in the first case is due to the set of contributions from caught external electro-magnetic interferences partial efficiency of the reset operation and flicker noise. All of them are not present after CDS processing. This fact underlines the usefulness of the CDS processing in increasing signal to noise ratio improving and facilitating the extraction of physical signals.

6.6.3 Charge Collection Efficiency and Cluster Signal Distribution

The current paragraph presents selected results on properties of charge collection and charge spreading, referred to distribution of signals onto the contiguous pixels, measured with the MIMOSA chips. Figure 6-21 shows a typical form of the dependence of the mean cluster signal for the MIMOSA I chip upon the cluster size. The cumulative sum of signals, where signals of pixels involved in the cluster formation around the seed pixel are summed according to the descending order of their amplitudes, is an ascending function of the cluster multiplicity. This plot illustrates charge sharing mechanism in the MIMOSA I chip obtained in tests with a ^{55}Fe source. The seed pixel constitutes approximately only one third of the total signal found on the cluster of 5×5 neighbouring pixels. The curve was obtained applying the cut of five and ten on the seed pixel and 3×3 pixel cluster SNR, respectively. The form of this curve depends on the version of the MIMOSA chip. Faster saturation occurs for thinner epitaxial layers and for pixels with multiple charge collecting diodes.

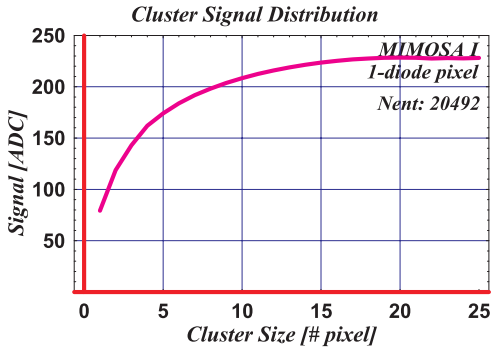

Figure 6-21: Mean cluster signal as a function of the cluster size for the single diode pixel configuration in the MIMOSA I chip.

6.6.3.1 Soft X-ray spectroscopy

Figure 6-22 shows the signal height distributions for photons emitted by an ^{55}Fe source measured on the central pixel and for clusters sizes of 2×2, 3×3 and 5×5 pixels for each reconstructed hit for the single diode pixel configuration in the MIMOSA I chip. Each graph in this figure shows a cumulative sum of signals. The first histogram was made for signals measured on the central pixel. The next histograms were obtained for the seed pixel and its closest 3, 8 and 25 neighbours, while the succeeding pixels involved in the cluster formation were chosen according to the descending order of their amplitudes. It is noticeable, that the

signal peak gets shifted, approaching the small peak position of the full collection efficiency when the cluster size increases. This observation indicates high efficiency of the charge collection from the epitaxial layer for the MIMOSA I chip. Comparably high collection efficiency was observed for other chips from the MIMOSA family with exception of MIMOSA III. In the case of MIMOSA III, the clustering did not show any improvement in approaching to the full charge collection.

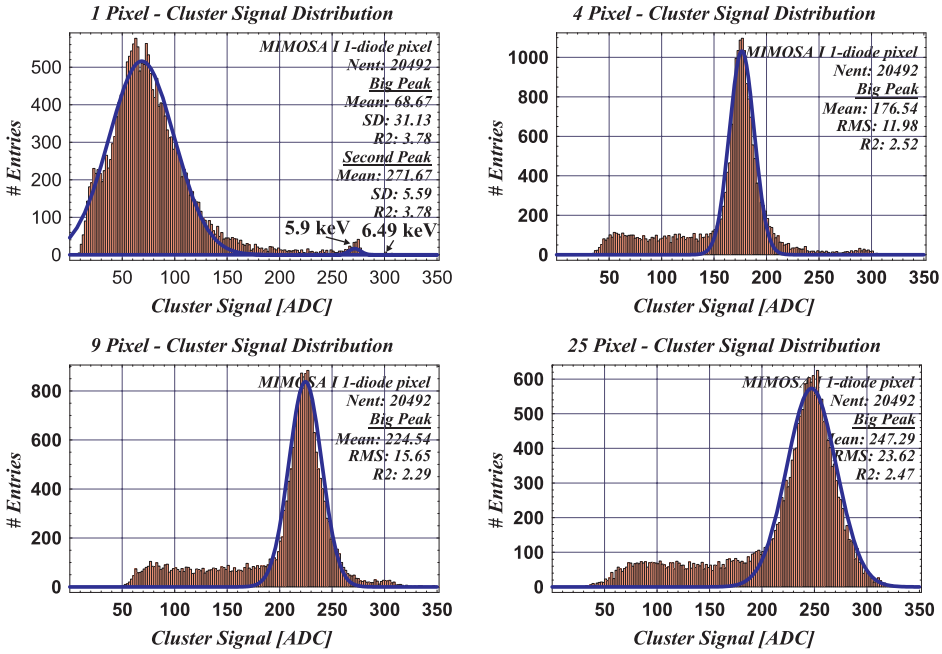

Figure 6-22: Signal height distribution for photons emitted by an ^{55}Fe source measure on the central pixel and for cluster of 2 × 2, 3 × 3 and 5 × 5 pixel multiplicities for each reconstructed hit for the single diode pixel configuration in MIMOSA I.

It was observed that only a small portion of the charge generated in the epitaxial layer is in average collected and results in signal of a reconstructed cluster. The main peak measured on the central pixel remained nearly unchanged in its position regardless the size of a cluster. It did not approach the peak of the full collection efficiency. Moreover, the distinction between the noise and signals of low amplitudes was difficult since there was no visible separation between them in data histograms. Figure 6-23 shows distributions of the acquired signals for each reconstructed hit. For each case, i.e. for each reconstructed hit, signal distributions for the seed pixel and for summed contributions from the seed pixel and its 2, 7 and 19 neighbours are shown, respectively. The neighbouring pixels, which signals are summed with

the signal on the seed pixel, are chosen ordering consecutively the highest detected signal. Plots in Figure 6-23 take into account a staggered layout of arrays of pixels in the MIMOSA III chip and the hit were identified applying cut on SNR of 5 for the central pixel and of 7 for the 19-pixel cluster signal. The results obtained with X-ray photons for the MIMOSA III chip, featuring only 2 μm of the epitaxial layer, suggest that charge collection is very inefficient for this chip. As one of possible hypothesis, the obtained test results may be explained by the minority carrier lifetime drastically decreased in the epitaxial layer in this case. The technological process of the epitaxial layer growth is conveyed at an increased temperature of a few hundred degrees centigrade.

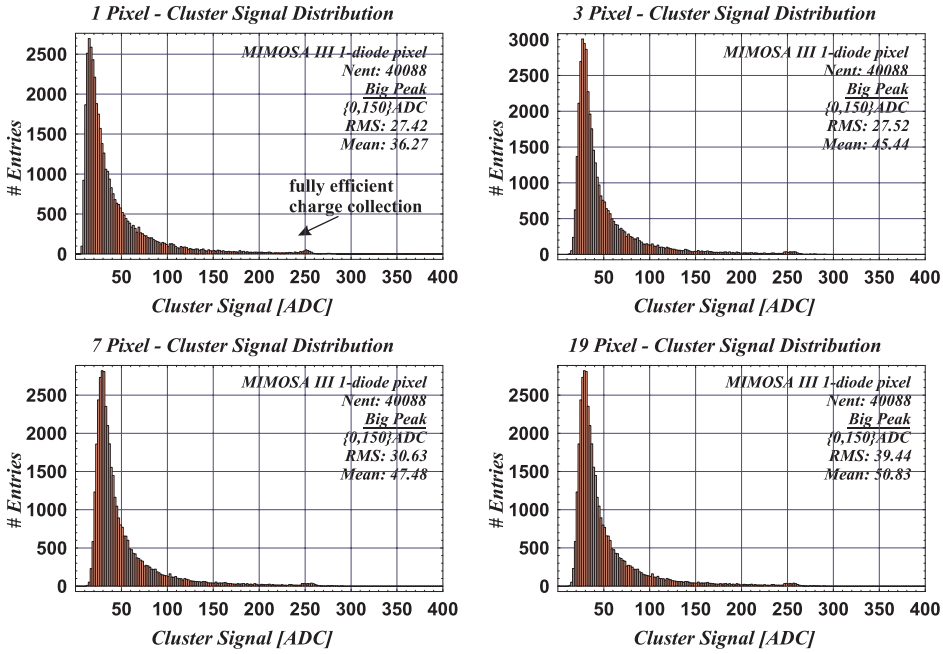

Figure 6-23: Signal height distribution for photons emitted by an ^{55}Fe source measure on the central pixel and for clusters of 3, 7 and 19 pixels of a staggered geometry pixel arrays for each reconstructed hit for the single diode pixel configuration in MIMOSA III.

Thus, the effective doping of this newly grown layer can be affected by species diffusion from the highly doped substrate. If this is the case, the low doping, which translates to the long minority carrier lifetime, cannot be guaranteed for the epitaxial layer. The generated charge recombines before electrons reach the region close to the diode, from where they are collected. Another hypothesis explaining poor charge collection in the case of the MIMOSA III chip accounts for creation of other sinks for the generated charge than n-

well/p-epi diodes. Potentially such a role could play as a function of the voltage bias applied shallow n^+-type diffusions for source and drains of the NMOS transistors in the pixel area. The presented hypotheses could be confirmed if the doping profile in the epitaxial layer can to be measured.

Figure 6-24 presents three distributions for the single and four diode pixel configurations in MIMOSA I and for the single diode pixel configurations in the MIMOSA III and IV.

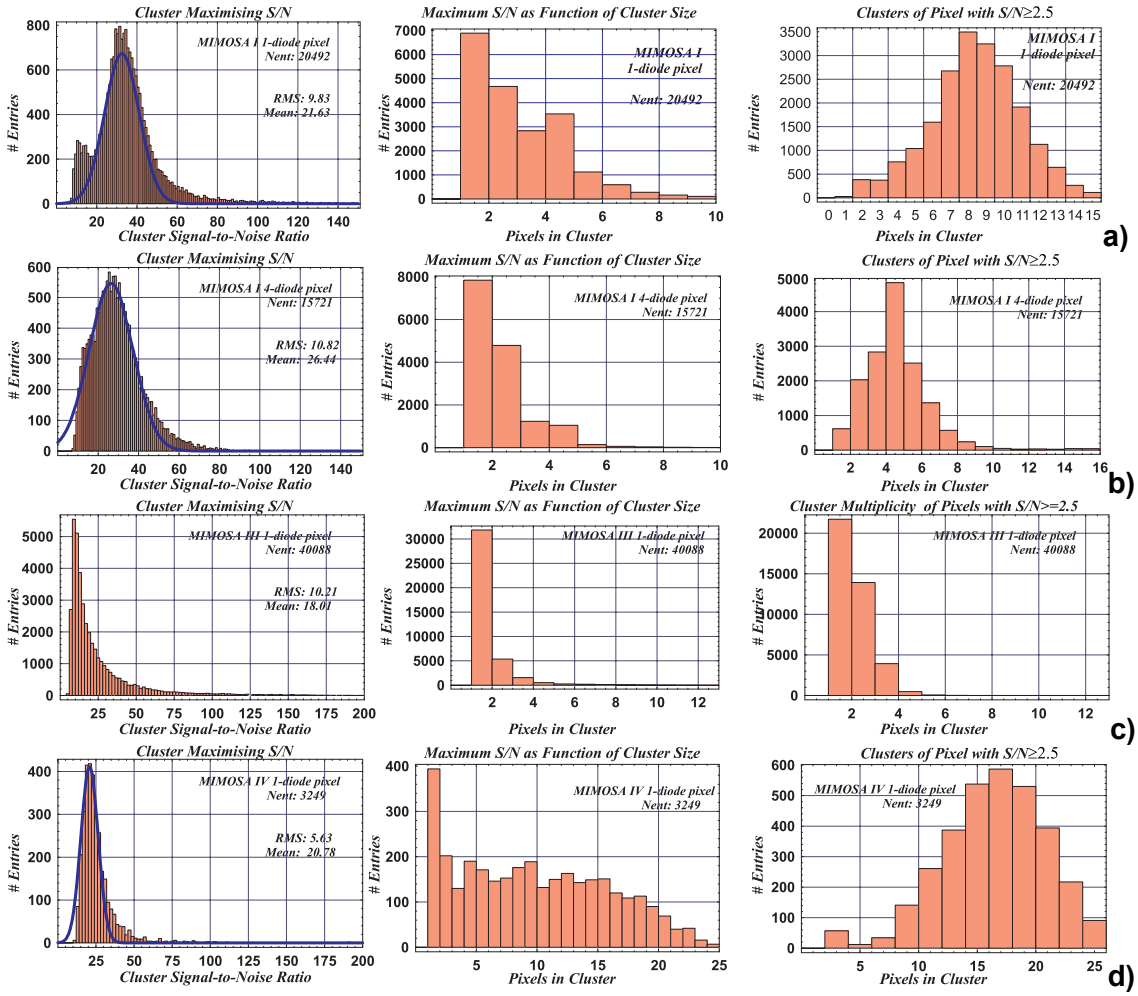

Figure 6-24: Signal-to-noise ratio distribution for clusters with maximised SNR, distribution of the number of pixels involved in cluster configuration maximising its S/N, cluster multiplicity distribution with all the neighbouring pixels exhibiting S/N equal or superior to 2.5 for (a) single diode pixel configuration in MIMOSA I, (b) four diode pixel configuration in MIMOSA I, single diode pixel configurations in (c) MIMOSA III and (d) MIMOSA IV.

The most left hand side graphs show distributions of a SNR for clusters of pixels, where the

number of involved pixels is chosen to maximise SNR of the cluster. The middle graphs show distributions of the number of pixels involved in such a cluster construction, and the most left hand side presents cluster multiplicity distribution, where only these neighbouring pixels are taken into account which exhibit SNR equal or superior to 2.5.

In the case of MIMOSA I, the signal is present on more than one pixel, the charge is widely spread and the strong signal is detected on the neighbours of the seed pixels. The distribution of the SNR shows a visible separation between the measured signal and the noise level. The maximum SNR is achieved frequently for the cluster multiplicity of even four. The distribution of the number of pixels, exhibiting SNR equal or greater than 2.5, maximises at the level of eight or nine neighbouring pixels.

In the case of MIMOSA III, the signal is present only on one pixel in most cases and only very low signals were detected on the contiguous pixels. The SNR distribution shows that there is no visible separation between the measured low amplitude signal and the noise level. The small cluster multiplicity can suggest fast recombination in the epitaxial layer, and only the charge liberated close to the collecting diode is collected.

In the case of MIMOSA IV, which is the chip fabricated on the non-epitaxial of increased resistivity substrate, the signal is present on many pixels. The cluster size reaches frequently the size of 5×5 pixels. The maximum of the distribution of the number of pixels obtained including pixels exhibiting SNR equal or greater than 2.5, falls in the region between 15 and 20 pixels.

6.6.3.2 Charge Distribution

To measure the charge density distribution for different pixel designs, a two-dimensional density function of the collected charge within a set of pixels in the cluster as a function of the distance from the X-ray photon impact was constructed. The function was built by plotting the projection of all the reconstructed clusters on the common plane sector. The centre of each cluster, representing the photon impact position, was calculated by a simple centre-of-gravity method. For each estimated cluster, the calculated impact positions were superimposed in the middle of the plot on the common plane sector. Then, signals of all pixels constituting the cluster were summed. The grid used for signal summation was defined tighter than the pixel pitch. Signals were summed in positions reckoned by the amount of the

shift to achieve the middle point of the plot by the centre of gravity of the cluster charge. Finally, the obtained numbers were normalised to the highest sum present in the plot. The resolution of this projection plot was set to 1.8 μm for all MIMOSA chips apart the MIMOSA III chip, for which it was increased to 0.7 μm. The derived density function for collected charge is an equivalent of the Modulation Transfer Function (MTF). The MTF function is commonly used in visible light applications for determining the resolution of the imaging device. It characterises the response of an image sensor to changing spatial frequencies [102]. The MTF function of the MAPS detector can be expressed as a product of the MTF_{geo} function depending on the geometry of the sensor and the MTF_{dif} due to the charge carrier diffusion

$$MTF_{tot} = MTF_{geo} \cdot MTF_{dif} . \tag{6-15}$$

Formula (6-15) in contrast to CCDs doest not include the MTF contribution due to the incomplete charge transfer in the device. In the case of the square and homogeneous pixel layout of the detecting array, which is characterised by the fill factor of 100%, the MTF contribution due to the detector geometry is given by

$$MTF_{geo}(f) = \left[\frac{\sin(\pi \Delta x f)}{\pi \Delta x f} \right]^2 , \tag{6-16}$$

where f is a spatial frequency, Δx is a pixel pitch. The diffusion part of the MTF function [103] accounts for the portion of the electrons generated in the detector active volume, which have to diffuse to the potential wells in order to be collected. It allows to take into account effects of many charge carriers which are not collected at all because they recombine or diffuse in any other direction than those directions of the potential wells, or charge carriers which are collected by any other pixel than this one which is located exactly above the generation point.

The charge sharing between neighbouring pixels in the MAPS detectors was analysed inspecting the obtained charge density function. The results are shown in Figure 6-25, Figure 6-26 and Figure 6-27 for MIMOSA I, MIMOSA II and III, and MIMOSA IV, respectively. As expected, the charge in the MIMOSA I chip is most concentrated for the four-diode pixel configuration. In the case of the MIMOSA II chip, the charge collected with the single diode pixel configuration was also less spread out than for the corresponding design in the MIMOSA I chip due to the thinner epitaxial layer. The smeared humps on the MTF

functions in the projection plots along the X-axis results from imperfections in the read-out electronics.

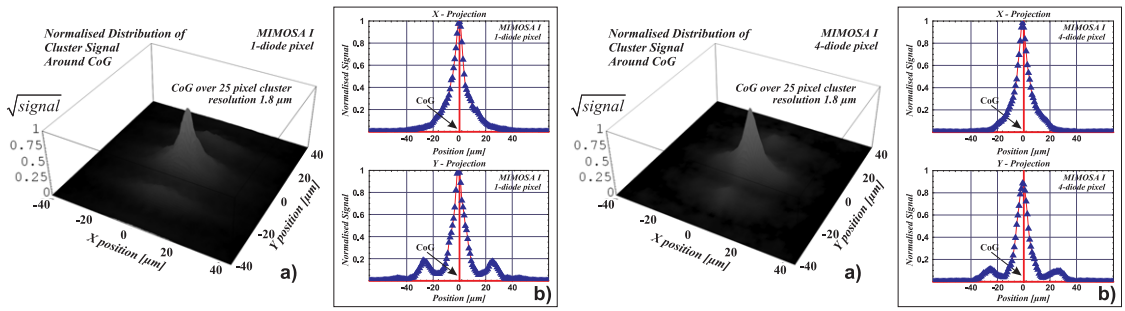

Figure 6-25: (a) Projection of the cluster signal around the cluster centre and (b) related projections along X and Y-axes for the single (left part) and four diode configurations (right part) in the MIMOSA I chip.

The X-axis is aligned with the read-out direction in the rows of the array under test, thus it can also be identified with the sequence at which pixel signals appear in the output data read-out in series. The amount of smearing on the MTF function is dependent upon the read-out clock frequency and is accredited to the lagging of the read-out channel time response.

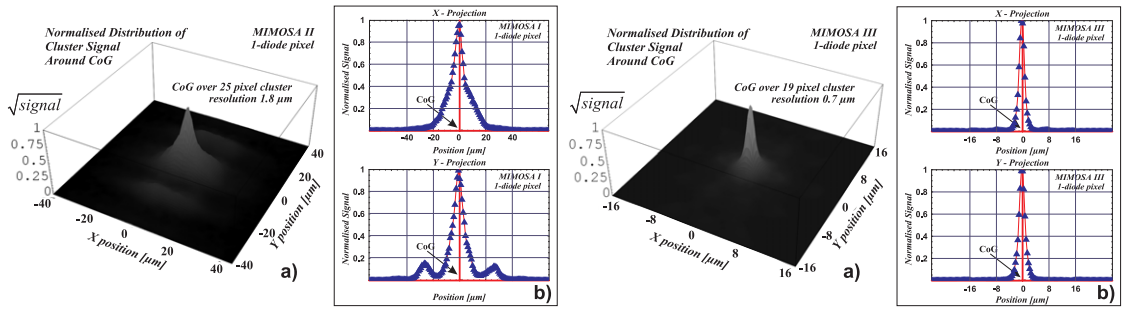

Figure 6-26: (a) Projection of the cluster signal around the cluster centre and (b) related projections along X and Y axes for the single diode configuration in the MIMOSA II (left part) and MIMOSA III chips (right part).

In the case of the MIMOSA III chip the charge sharing mechanism seems to be inefficient, the humps on the MTF function are completely eliminated as it can be noticed in both projection plots along X and Y axes in the left hand side part of Figure 6-26. It is apparent, that the diffusion dependent part of the MTF function is a steeply decreasing function of the distance, which is an inverse of the spatial frequency. The charge sharing mechanism is almost not observable and the average distance, according to Figure 6-26, from the collecting

diode from which the liberated charge is collected is less than the half of the pixel pitch. The widest charge spreading is observed for the MIMOSA IV chip. The MTF function exhibits clear humps on both sides of the central peak, which means that the diffusion dependent part of the MTF function is a function of widely spread arms.

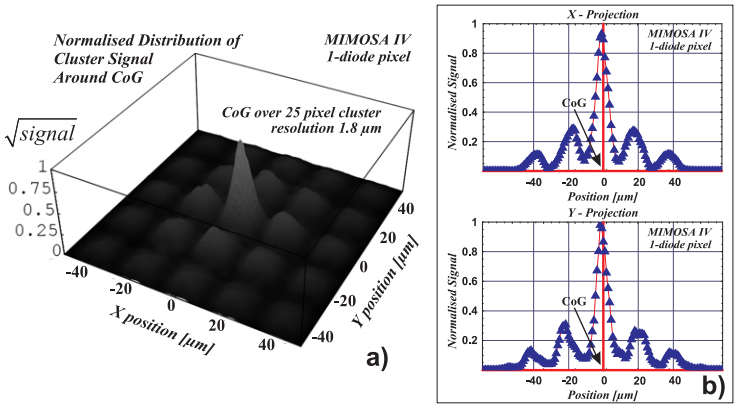

Figure 6-27: (a) Projection of the cluster signal around the cluster centre and (b) related projections along X and Y-axes for the single diode pixel configuration in the MIMOSA IV chip.

The humps are easily distinguishable, which means that the problems with time response of the read-out electronics have fully been eliminated. The charge collected with the single diode pixel configuration was widely spread due to the practically unlimited thickness of the active volume in this chip.

6.6.4 Calibration of the Charge-to-Voltage Conversion Gain

6.6.4.1 Calibration with Soft X-rays

In order to calibrate the charge-to-voltage conversion gain for the MIMOSA chips with soft X-ray photons, the calibration procedure presented in Chapter 2.3.3 was used. The precise calibration of the conversion gain, carried out in the identical test set-up as the one used throughout the tests with charged particles from the beam, allowed to express the collected charge and other parameters related to the measured detector performances in absolute units i.e. number of charge carriers. The example results obtained in spectroscopy of photons emitted by a ^{55}Fe source are shown in Figure 6-28. The left hand histograms in this figure comprise all signals which magnitudes were high enough to surpass the assumed threshold for cluster SNR. All graphs include only signals measured by the central pixel in the

recognised clusters. The results were obtained for different pixel configurations for three chips from the MIMOSA family.

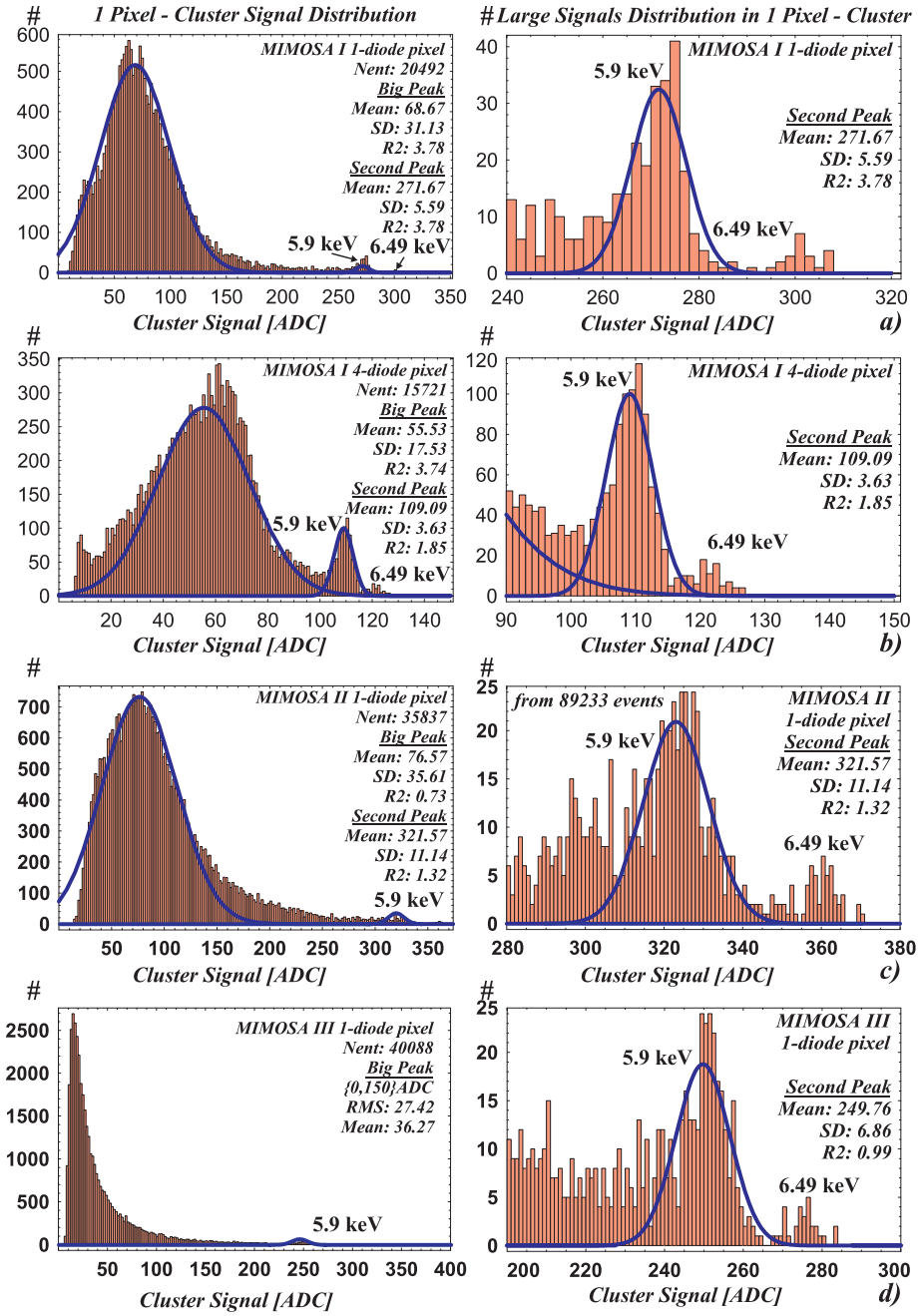

Figure 6-28: Results of X-ray spectroscopy using an ^{55}Fe source with the MIMOSA chips; (a) single diode pixel configuration in MIMOSA I, (b) four diode pixel configuration in MIMOSA I, (c) MIMOSA II, (d) MIMOSA III; Right hand histograms show the peak referred to as reflecting 100% collection efficiency which originates from the photons converted near the diodes.

The right hand histograms show the part of the measured spectra containing only entries at the highest signals. This part assumes a shape of two clearly unequal amplitudes peaks. The position of the second peak is shifted approximately 10% towards higher signals with respect to the position of the higher peak. Thorough analysis shows no charge collected onto the adjacent pixels to the central pixels for the events from both peaks. The ratio of entries number in both peaks as well as their mutual positions allow to identify two emissions modes from the ^{55}Fe source. Their presence reflects 100% collection efficiency for a small sub-sample of photons converted near the charge collecting diodes, and the position of the peak for 5.9 keV photons was used to measure the conversion gain and consequently the total value of the conversion capacitance and ENC. The obtained results are summarised in Table 6-14. This table includes results for single and four diode pixel configurations from the MIMOSA I chip, single and two diode radiation tolerant configurations from the MIMOSA II chip and unique single diode configuration from the MIMOSA III chip.

Table 6-14: Charge-to-voltage conversion gain, total conversion capacitance and noise for the MIMOSA I, II and III chips.

MIMOSA I	**1-diode**	**4-diodes**
Conversion gain	14.6 μV/e$^-$	6.0 μV/e$^-$
Total node capacitance (@ V_{DD}=5V)	10.9 fF	26.6 fF
Noise ENC (CDS 1.25 MHz @ T=-20°C)	15 e$^-$	31 e$^-$
MIMOSA II	**1-diode rad-tolerant**	**2-diodes rad-tolerant**
Conversion gain	22.9 μV/e$^-$	17.5 μV/e$^-$
Total node capacitance (@ V_{DD}=3.3 V)	7.0 fF	9.1 fF
Noise ENC (CDS 2.5 MHz @ T=+20°C)	16 e$^-$	18 e$^-$
MIMOSA III	**1-diode rad-tolerant**	
Conversion gain @ W/L=3.8 μm/0.57 μm and 40 μA bias current (source follower)	10.5 μV/e$^-$	
Total node capacitance (@ V_{DD}=2.5 V)	12.6 fF	
Noise ENC (CDS 10 MHz @ T=0°C)	8 e$^-$	

The charge-to-voltage conversion gain expressed initially in the ADC units corresponding to a single electrons was converted to units of the voltage shift for a single electron at the output of the source follower transistor after determination of the total voltage gain of the read-out channel.

6.6.4.2 Statistical Method of Calibration

Calibration of the charge-to-voltage conversion gain for the MIMOSA chips using the method exploiting the Poisson statistics of the shot noise was done according to the calibration procedure described in Chapter 2.3.2. The method was successfully applied to the MIMOSA III chip, realised in a deep sub-micrometer process, for the experimental verification of the noise optimisation procedure described in Chapter 2.4.2. In the MIMOSA III device, one test array was foreseen for tests aiming at the experimental verification of the noise level dependence on the gate length of the source follower transistor in a pixel. Particularly important was to demonstrate the increase of the measured noise for the minimum gate length of this transistor. The test array is subdivided into four 128 × 30 pixel sub-matrices. Each sub-matrix features the source follower transistor of different dimensions: W_1/L_1=3.2/0.27, W_2/L_2=3.4/0.37, W_3/L_3=3.6/0.47, W_4/L_4=3.8/0.57, while the width of the transistor has a minimum value for a given transistor length obtainable for an enclosed gate layout. The details on the layout of the MIMOSA III chip and the test array arrangements are given in Appendix-C.

The charge-to-voltage conversion gain was determined for pixels in every single sub-matrix using a red light LED diode used as an excitation source. Controlling the current conveyed by the diode varied the light intensity and the light signal was integrated over the time interval equal to the read-out time of one full frame. The MIMOSA III chip was clocked at 5 MHz, which translates to the integration time of 6.62 ms. The total number of 12 illumination levels was used to generate plots of transfer curves of the signal variance versus the mean signal as required in the calibration method. The statistics calculations were done over N=140 events taken for each level of light intensity. Figure 6-29 shows results of the charge-to-voltage gain calibration obtained according to the statistical method for the MIMOSA III chip. Histograms shown on the left hand side of this figure show distributions of the conversion gain for individual pixels. The pixel-to-pixel variation of this quantity can be determined for the examined sub-matrices from the width of corresponding distributions after deconvolution from errors of the gain estimation for each individual pixel. The right hand side graphs show examples of fits for a single pixel picked in a random way from each calibrated sub-matrix. Calculation of errors on all the signal variances referencing to each measured mean signal was required to perform correctly a fitting session. This calculations

were possible, because the variable used for plotting was already a variance obtained by sampling N=140 images. Thus, the classical formula for the standard error σ_y on a standard deviation σ was used

$$\sigma_y = \frac{\sigma}{\sqrt{2(N-1)}}, \tag{6-17}$$

and linear fits with high goodness were obtained. The charge-to-voltage conversion gain for individual pixels is determined from the slope of each line. The plotted straight lines were shifted down to intercept the origin point of the graph axes. The value of this shift determines the irreducible read-out noise level, which corresponds to the operation of the chip in darkness without any excitation source of light.

The conversion gain can also be determined, limiting the measurements to one illumination level, as the ratio of the signal variance and the mean signal. The numbers written at the vicinity of symbols in Figure 6-29 give corresponding values of the conversion gain estimated at each illumination level. A relatively large variation of the obtained numbers may have several origins. Beside the need for the large data statistics acquired for each illumination level, which allows minimising measurement errors, very good stability of the light source is particularly important during the experiment. Generally, the use of the transfer curve in the form of the linear fit rather than single illumination measurements is justified for practical reasons. The summary of the obtained results is given in Table 6-15. This table includes results for pixel configurations featuring different dimension of the source follower transistor in the MIMOSA III chip. Accordingly to the calibration method with soft X-ray photons, determination of the total voltage gain of the read-out channel allowed to express the charge-to-voltage conversion gain at the output of the source follower transistor in the units of the voltage shift corresponding to a single electron.

Table 6-15: Charge-to-voltage conversion gain for the MIMOSA III chip.

Source follower - enclosed gate - (W/L)	**Conversion gain [ADC/e$^-$]**	**Total voltage gain [ADC/V]**	**Conversion gain [μV/e$^-$]**	**Individual pixel gain mean error**	**Pixel-to-pixel gain dispersion**
3.2 μm / 0.27 μm	0.1389	8300	16.73	σ =5.0%	σ =5.2%
3.4 μm / 0.37 μm	0.1233	8300	14.85	σ =4.8%	σ =4.8%
3.6 μm / 0.47 μm	0.1070	8300	12.89	σ =5.2%	σ =3.9%
3.8 μm / 0.57 μm	0.0902	8300	10.87	σ =5.2%	σ =3.6%

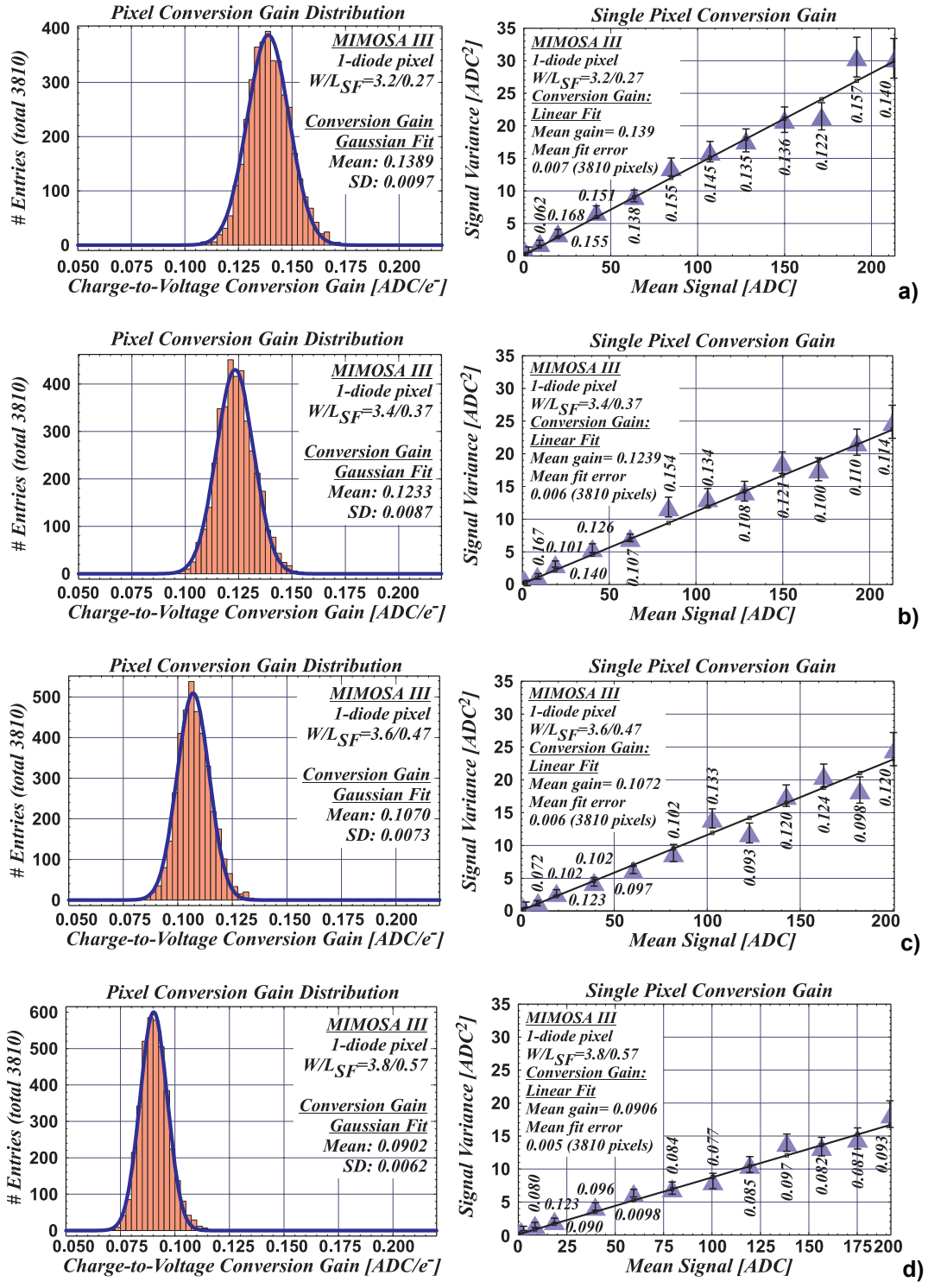

Figure 6-29: Results of charge-to-voltage gain calibration for the MIMOSA III chip obtained by means of the statistical method for different dimensions W/L of the source follower transistor: (a) 3.2/0.27, (b) 3.4/0.37, (c) 3.6/0.47, (d) 3.8/0.57.

The pixel-to-pixel variation of the conversion gain was determined at the level of a few percent only.

Precise estimation of the charge-to-voltage conversion gain for each sub-matrix for the MIMOSA III chip allowed to evaluate pixel noise performance as a function of the dimensions of the source follower transistor. Variation of the irreducible noise was measured for pixels in each sub-matrix in the MIMOSA III chip operated at 5 MHz of the read-out clock frequency for two values of the capacitive load of the source follower. An external digital signal was used for switching between the load capacitors of 3.2 pF and 9.8 pF. The noise was estimated as the sample variance for 140 events recorded after the pedestal and common mode shift corrections. Figure 6-30 shows graphs of the measured noise expressed in ENC as a function of the source follower transistor gate length for the MIMOSA III chip.

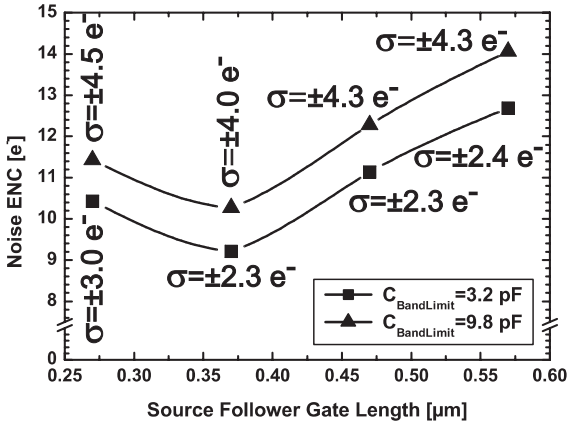

Figure 6-30: Variation of measured noise ENC as a function of the gate length of the source follower transistor for the MIMOSA III chip operated at 5 MHz of the read-out clock frequency.

It is noticeable that distinct minima are present in both curves in Figure 6-30 for the source follower transistor gate length of 0.37 μm. Despite the lower value of the charge-to-voltage conversion gain, the noise level is approximately 10% lower at this gate length than for the minimum one. The use of the higher capacitance value to load of the read-out line leads to a further 10% decrease of the read-out noise. Although the results obtained experimentally do not fully reproduce prior noise estimation at the design stage of the MIMOSA III chip, the noise optimisation procedure leading to the use of non-minimum gate length transistor as the source follower is validated. Some discrepancy between the theoretically obtained numbers and experimental results may originate in an inability to operate the detector under

the nominal bias conditions. The detector was operated at increased bias current of the source follower transistor ranging from 45 μA to 55 μA and the read-out clock frequency was decreased to 5 MHz. The problem was caused by an error in the digital part, which fortunately did not prevent utterly the detector to be operational. The pixel-to-pixel variation of the measured noise in the range of 2.3 e^- to 4.5 e^- is qualitatively much higher than the previously stated 5% of the corresponding pixel-to-pixel variation of the charge-to-voltage conversion gain.

6.7 Evaluation of Radiation Hardness

Radiation hardness of the MAPS devices is an important issue for applications at the radiation environments of future particle and nuclear physics experiment. A very high interaction rate and also beam induced radiation background expected in such an environment translates into several strong requirements on the radiation hardness of the detector. This is particularly true for those located close to the interaction point.

Although CMOS APS are getting to be prevalent, very few data exist on their degradation due to irradiation. Since radiation hardness is beyond the scope of interest for commercially produced digital cameras, those available data concern mainly radiation effects under space environment [104, 105, 106]. First experiments on total dose effects showed that the dark current is the most affected parameter under irradiation. However, it was observed that radiation-induced leakage current decreases after a thermal annealing procedure. On the other hand, it was observed that even when the APS devices were implanted on radiation hardened technologies; they equally suffer from leakage current degradation under proton irradiation [107].

In the case of CMOS devices for charged particle tracking, an increase of leakage currents of the charge collecting diode may induce undesired effects on the device operation, like shorter saturation time and increased shot noise. The need of preserving an efficient charge collection from the epitaxial layer underneath the electronics sets additional constrains.

The immunity of the MAPS detectors to different kinds of radiation was the subject of intensive tests using the MIMOSA I, II and III prototypes. The chips were characterized before and after irradiation, by measuring the leakage current as well as the charge collection

properties and the charge-to-voltage conversion gain with a ^{55}Fe X-ray source. They were exposed to 30 MeV/c protons with fluencies up to 5×10^{11} p/cm^2, 10 keV X-ray photons up to the total dose of 400 krad and neutrons with fluencies up to 1×10^{12} n/cm^2 (1 MeV neutrons equivalent) [108]. Irradiations were performed in several institutions using the irradiation test facilities at the Institut für Experimentelle Kernphysik, Universität Karlsruhe, Germany for proton and X-rays, the European Organisation for Nuclear Research (CERN), Geneva, Switzerland for X-ray irradiations and the Commissariat à l'Energie Atomique (CEA) and the Joint Institut for Nuclear Research (JINR), Dubna, Russia for neutron irradiations.

6.7.1 Proton Irradiation

Proton irradiations were carried out with a 30 MeV/c proton beam from the cyclotron. Two prototypes, i.e. MIMOSA I and II, were exposed to irradiations under bias and clocked read-out to reduce ionisation effects. The maximum proton fluence in this series of tests was set to 5×10^{11} p/cm^2. This corresponds to an ionisation dose of about 50 krad and to an atomic displacement effect i.e. bulk damage equivalent to 10^{12} of 1 MeV equivalent n/cm^2. Under this irradiation condition, the major effect anticipated on the pixel device was the one due to bulk damage, resulting in decrease of a minority carrier lifetime in the moderately doped p-type epitaxial layer. The charge collection through thermal diffusion from the undepleted epitaxial layer is relatively slow. According to the measurements, presented in Chapter 6.4, the charge collection occurs within a typical interval in the order of 100 ns, while the minority carrier lifetime for the doping level about 10^{15} cm^{-3} is estimated to be less than 10 μs in absence of irradiation. Therefore, the decrease of the minority carrier lifetime may influence the charge collection efficiency and consequently the signal amplitude, which may accordingly be decreased. Moreover, the n-well/p-epi diode leakage current may increase, due to the increase of the junction generation-recombination currents.

The damage of the irradiation was evaluated by studying the signal generated by a ^{55}Fe X-ray source before and after exposure. The photon pulse-height spectroscopic distribution measured with MAPS detectors is characterised by the presence of two peaks, as it can be seen in Figure 6-34. The broad low amplitude peak corresponds to photons converted in non-depleted epitaxial layer, while the small peak of higher signal amplitude corresponds to

the photons converted in a region around the junction of the charge collecting diode. The position of this small peak is used to determine the device gain calibration. The charge-to-voltage conversion gain of the devices exposed to the proton beam was not modified, while the signal amplitude was shifted towards lower values. Figure 6-31 shows a decrease of the relative signal amplitude measured on the single and four diode pixel configurations in the MILMOSA I chip and single and in the single and two diode pixel configurations in the MIMSOA II chip. The signal amplitude was measured as a position of a broad photon peak as a function of the proton fluence for the central pixel only and summing up contributions within the cluster of 2×2 contiguous pixels exhibiting highest signals. Charge losses of up to 45% were observed after a fluence of 5×10^{11} p/cm^2.

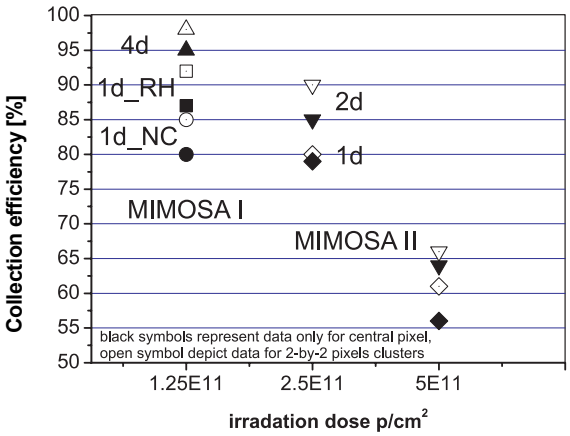

Figure 6-31: Collected charge, normalised to the initial sample measurements, after irradiation with protons for two prototype chips MIMOSA I and II, for different pixel configurations (1, 2 and 4 diodes) implemented inside.

In parallel to the charge losses evaluation, leakage current was monitored as a function of the irradiation dose. The related increase of the average leakage current was measured indirectly as a voltage change rate on the device charge-collecting node. The example results are shown in Figure 6-32 as a function of temperature for the single and two diode pixel configurations in the MIMOSA II chip. Despite the strict observation of the radiation tolerant layout rules in the design of this chip, the increase of the leakage current was significant, reaching the factor ranging from 4.5 to 6 times after a fluence of 5×10^{11} p/cm^2 correspondingly for two pixel configurations implemented on the chip. It is characteristic of the leakage current behaviour that the increase does not exhibit a direct proportionality to the number of parallel diodes, suggesting other sources to contribute to the measured leakage

current. This additional increase of the leakage current could potentially be induced by the ionisation dose connected with the proton exposure.

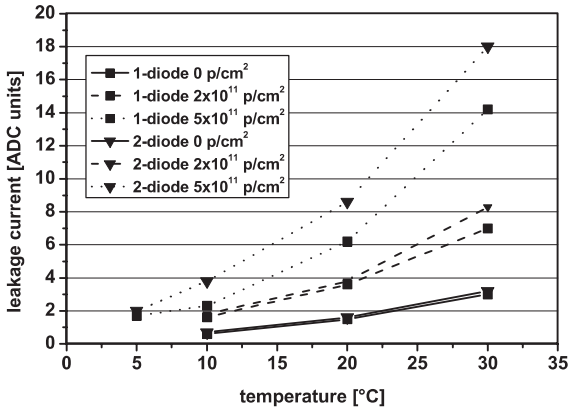

Figure 6-32: Increase of leakage current after irradiations with 30 MeV/c protons measured as a function of temperature for MIMOSA II prototype.

6.7.2 Neutron Irradiation

Genuine bulk damages were investigated by irradiating the sensors with a fast neutron beam peaked at 1 MeV. Unlike with protons, the bulk effects are here not overlaid with the interface states modification and the trapped charge induced by all kinds of ionisation. For these tests, special care was taken to keep the ionisation dose from the background of high-energy photons to a negligible level. The ionising dose corresponding to a neutron fluence of 6×10^{11} was measured to be negligibly low below 1 krad. Figure 6-33 shows obtained results for the single and four-diode pixel configuration in the MIMOSA I chip irradiated with a neutron fluence of up to 10^{12} n/cm^2. Figure 6-33a traces results on the change of the leakage current and electronic noise expressed in ENC as a function of neutron fluence. The measurement were done at 0°C. The one standard deviation pixel-to-pixel variation of the leakage current is marked as the wingspan of error bars at each measurement point, while the noise value is presented as numbers close to the symbols. It is worth noticing that both, i.e. the leakage current and electronic noise remain unchanged up to the highest neutron fluences experienced. Figure 6-33b shows neutron fluence dependence of the number of collected charge carriers on the central pixel, 2 × 2 pixel and 3 × 3 pixel clusters for the single and four diode pixel configurations in the MIMOSA I prototype. The charge losses become significant in the case of the single diode pixel configuration reaching 33.8% of the charge

loss after a neutron fluence of 10^{12} n/cm^2 relative to 100% of the collected charge assumed for the pixel of the non-irradiated chip. The four-diode pixel configuration show much higher immunity to the neutron irradiation, and only 5.8% of charge loss is observed after the exposure.

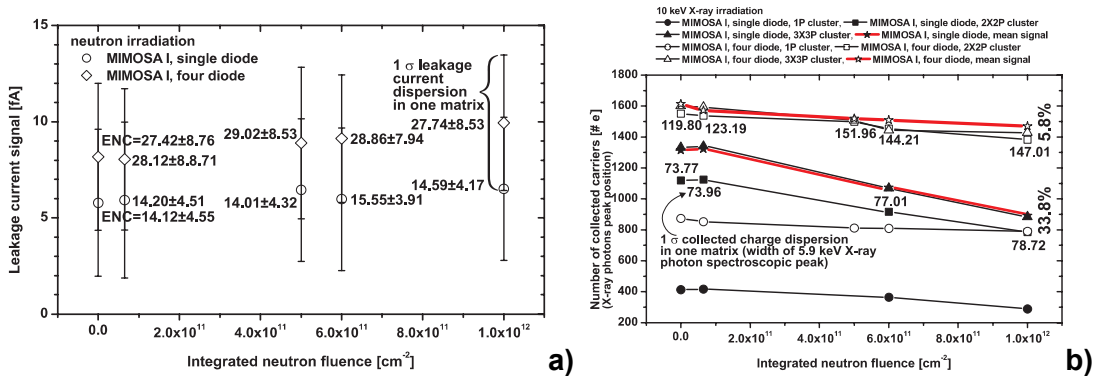

Figure 6-33: (a) Change of leakage current and electronic noise at 0°C, after irradiations with neutrons, (b) number of collected charge carriers on the central pixel, 2 × 2 pixel and 3 × 3 pixel clusters. Both graphs show data obtained for single and four diode pixel configurations in the MIMOSA I prototype.

According to these results, the losses of the collected charge can purely be attributed to the bulk damage caused by neutrons. The efficiency of the charge collection is directly related to the lifetime of the minority charge carriers in the epitaxial layer and the charge collection time. The decreased lifetime of electrons due to the neutron fluence translates to faster recombination of an excess charge. According to simulations, the four-diode pixel configuration is characteristic of more than two times shorter charge collection time with respect to the single diode one. This explains why, the four-diode pixel configuration starts only to suffer from charge losses after the highest neutron fluence of 10^{12} n/cm^2, while at this point the damaging effect is already very important for the one-diode pixel configuration.

6.7.3 Soft X-rays Irradiation

Irradiation tests were also performed using a 10 keV X-ray photons from an X-ray tube. The silicon bulk damage effects of such soft X-ray photons should be negligible. Figure 6-34 shows the signal pulse-height distributions for a ^{55}Fe X-ray excitation source measured with the single diode pixel configuration of the MIMOSA I chip. The left hand side histograms refer to the performance of the prototype before irradiation and the right hand side

histograms to irradiation with a dose of 100 krad. Two upper plots correspond to the signals measured on the seed pixel only, while two bottom plots show the summed contribution over the cluster of 2 × 2 pixels around it. The charges losses originate a displacement of the broad peak from the photons converted in the epitaxial layer. The displacement amounts to almost 6% at this relatively low dose, both for the seed pixel and for the 2 × 2 pixel clusters. This change could be partially explained by a change of the charge-to-voltage conversion gain experienced. This change is very slight. It amounts to less than 3% as seen from a small shift of the position of the calibration peak.

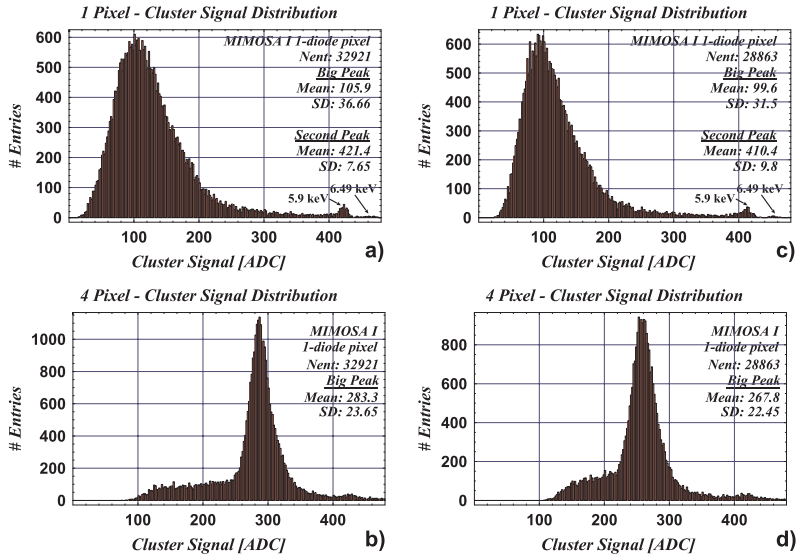

Figure 6-34: Sensor response to a ^{55}Fe X-ray source; Signal pulse-height distribution (a, b) before and (c, d) after a dose of 100 krad of 10 keV photons for (a, c) seed pixel and (b, d) for cluster of 2 × 2 pixel including the seed one for the MIMOSA I prototype.

Figure 6-36 shows X-ray dose dependence of the number of collected charge carriers on the central pixel, 2 × 2 pixel and 3 × 3 pixel clusters for the single and four diode pixel configurations in the MIMOSA I prototype. The charge losses are insignificant for either pixel configuration for the dose of up to 100 krad. However, it is noticeable from Figure 6-36 that in the case of the four-diode pixel configuration, the charge collection efficiency amounts to 100% up to the highest dose experienced, while in the case of the single diode pixel configuration, it starts already to be slightly degraded. This effect suggests that the charge collection from the epitaxial layer can also be affected by the ionising radiation, setting the dose of 100 krad as the threshold value. Preliminary data analyses for higher irradiation

doses of up to 400 krad for the MIMOSA I and II chips show indeed a substantial increase of the charge loss. The effect and the mechanism behind charge losses needs further studies.

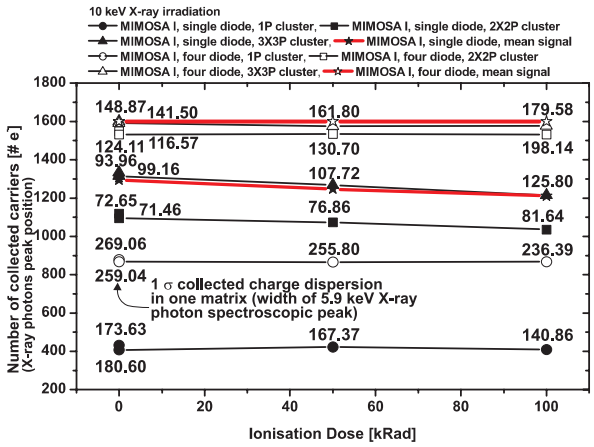

Figure 6-35: Number of collected charge carriers on the central pixel, 2 × 2 pixels and 3 × 3 pixels clusters for single and four diode pixel configurations in the MIMOSA I prototype.

The main effect expected due to the ionisation dose is an increase of the leakage current in the pixel. The leakage current was monitored as a function of the irradiation dose and showed a substantial increase. The increase of the average leakage current was measured indirectly as a voltage change rate on the device charge-collecting node. The example results are shown in Figure 6-36, which traces results on the change of the leakage current and electronic noise expressed in ENC as a function of ionisation dose. The measurement were done at 0°C.

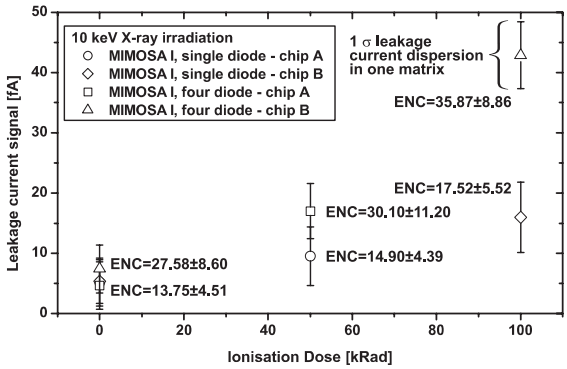

Figure 6-36: Variation of the leakage current and electronic noise measured at 0°C for the single and four diode pixel configurations in the MIMOSA I prototype.

The one standard deviation pixel-to-pixel variation of the leakage current is marked as the

wingspan of error bars at each measurement point, while the noise values are presented as numbers close to the symbols. It is noticeable that both, i.e. the leakage current and electronic noise increases with increasing ionisation dose. The total read-out noise increase originates mainly in the shot noise due to the increased leakages current.

The indirect method to measure the leakage current as a voltage drop on the device charge-collecting node for the time interval equal to the one full frame acquisition time cannot be taken as an absolute diode leakage measurement. The leakage current of the charge collecting diode may be compensated by contributions of other sources of leakage current present in the pixel, e.g. leakage current of the reset transistor channel. In order to provide a direct measurement, a special test structures made out of a few thousands of diodes were included in the MIMOSA III prototype. The layout of these diodes was identical to their layout on a pixel array and all were connected in parallel, however there were also unusual NMOS transistors (reset, source follower, readout switch) in the structure. This large number of diodes in parallel was needed because the measurement on individual devices exhibiting current of the order of femtoamperes would have faced serious technical difficulties. Figure 6-37 shows the leakage current referred to a single diode measured on this structure as a function of temperature before and after photon irradiation. The MIMOSA III chip was irradiated up to the total dose of 400 krad on the biased device and plus 400 krad accidentally under unbiased conditions. The measurements were done before irradiation, one day following photon irradiation, then 3 weeks later and after annealing at 100 °C for 24 hours. The complete sensor, using the indirect method to measure the leakage current in the array of pixels, exhibited only a factor 10 increase of the leakage current, whereas the increase observed on single diodes in the test structures was of the order of 200. The measurements shown in Figure 6-37 demonstrate also a strong annealing effect, observed even at room temperature. The leakage current decreases by 2.5 after 3 weeks of annealing at room temperature, then more extensive annealing at 100 °C results in further decrease by the factor of 5. Nearly the same quantitative effect was observed regardless the configuration and layout of the diodes in the measured test structures.

The problem of the irradiation induced diode leakage currents needs further investigation, since two methods of measurements give results, which show large discrepancy. There is no clear and simple explanation to the phenomena observed. One

hypothesis is based on a lack of n-well guard-rings around the test structures. These rings are present in the case of the main detecting arrays and they cut current paths from outside of the active volume.

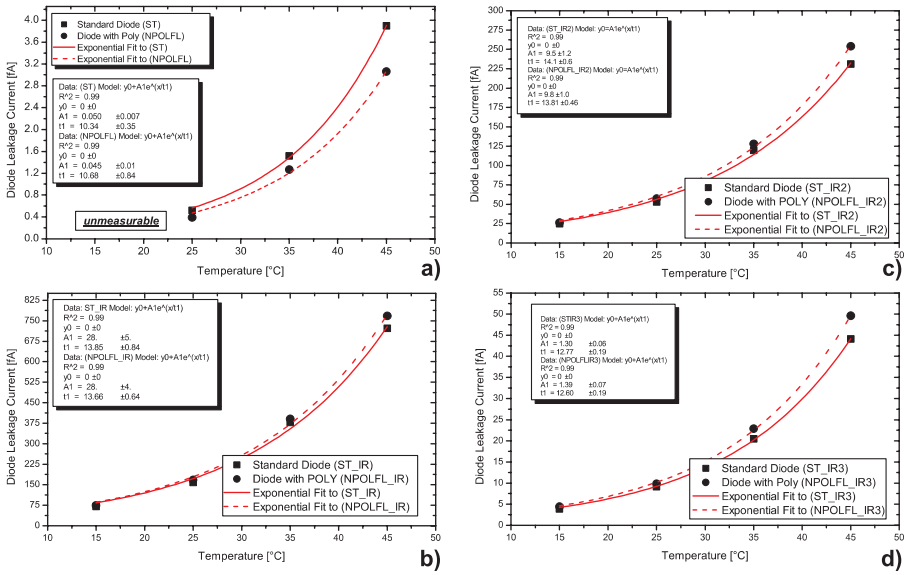

Figure 6-37: Variation of the leakage current related to a single n-well/p-epi diode (STANDARD and NPOL_FL) as a temperature function measured on MIMOSA III test structures (a) before irradiation and after 10 keV photons irradiations; (b) one day after, (c) 3 weeks of room temperature annealing, and (d) after additional 24 hours annealing at 100 °C.

The second hypothetic reason, explaining the excess of the measured leakage current can be the modification of the test structures layout with respect to the actual pixels. The space occupied by the transistors was liberated and filled with a p^+-type region and the test structures including their vicinity were not masked against filling with an n^+-type region and poly-silicon*. Only the surface of the main detecting arrays was protected against filling. The filling is done automatically by foundry over the unprotected regions in order to satisfy filling ratios for each layer according to the DRC† rules. The created floating n^+-type and poly-silicon regions together with omitted n-well guard-rings may provoke conductive paths conveying the charge to the diode in the test structures after ionising irradiations.

* The RXEXCLU and PCEXCLU (see IBM 0.25µm CMOS 6SF process design kit) layers were not extended over the test structures.

† DRC stands for Design Rules Checking performed during a VLSI chip design.

6.7.4 Summary of Irradiation Tests

A preliminary study of the radiation hardness of CMOS sensors adapted to charged particle tracking shows that losses of the collected charge from the epitaxial layer occur after proton, neutron and photon irradiation. The proton irradiation is accompanied by an increase of the leakage (dark) current. The similarity between the effects induced by protons and neutrons on the tested device suggest that the damage of the epitaxial bulk is responsible for these losses. A substantial increase of the leakage current, also observed after soft X-ray irradiation, seems to be linked to the interface state modification. A detailed study tracking the origin of these effects is needed. In particular, the consequence of the presence of a thick oxide and shallow trench isolation structures close to the n-well/p-epi junction should be evaluated. The understanding of the effects observed may benefit from a detailed device simulation. The effects observed do not reflect the ultimate potential of the technology concerned and several design improvement are to be tried. Some new charge collecting diode structures, with no thick oxide around junctions, were proposed as described in Chapter 2.3.2. Unfortunately, those implemented in MIMOSA III [87] were not functioning, which was possibly because of problems ensued in the fabrication stage. However, several other designs are being considered and one expects that within coming years substantial improvement will come out from the effort under way.

6.8 Tests with Charged Particle Beams

The response of the MIMOSA chips to charged particles traversing a MAPS sensor was studied in 15 GeV/c and 120 GeV/c pion (MIPs equivalents) beams from the CERN PS and SPS accelerators, respectively. For these tests, pixel detectors were mounted inside a high precision beam telescope and a small scintillation counter matching the physical dimension of the tested device and delivering a trigger. The detailed description of the test set-up is provided in Chapter 6.2.2. This chapter presents a detailed overview of the data analysis and its results for the MIMOSA I and II chips, the two prototypes from the MIMOSA family that were exposed to high-energy particle beams.

6.8.1 Collected Charge

The variation of the collected charge as a function of the cluster size is plotted in Figure 6-38 for the MIMOSA I and II prototypes. Pixels were successively added to the cluster in decreasing order of their signal amplitudes. The graphs in Figure 6-38 were done for the most probable values of the collected charge. They were obtained for peaks of the measured Landau-like distributions. The charge-to-voltage conversion gains were determined with 5.9 keV photons from a ^{55}Fe source, allowing to use absolute units of a number of electrons for amount of collected charge. The charge collected in the cluster was found to be in the range of 1000-1200 e^- and 300-400 e^- for MIMOSA I and II, respectively. The absolute amount of the collected charge is about 20% larger for the four diode pixel design in MIMOSA I and 10% higher for the two diode pixel design in the second chip with respect to the single diode pixel configuration in both chips. The charge produced by MIPs was spread over several pixels. About 90% of the total charge was concentrated within a cluster of 3 × 3 pixels and the charge spread appears to be limited to about 16 pixels per cluster for both pixel configurations in MIMOSA I and about 12 for MIMOSA II. The hit position reconstruction algorithm used later for determination of the intrinsic spatial resolution of the devices considered clusters of up to nine pixels (3 × 3 pixel clusters).

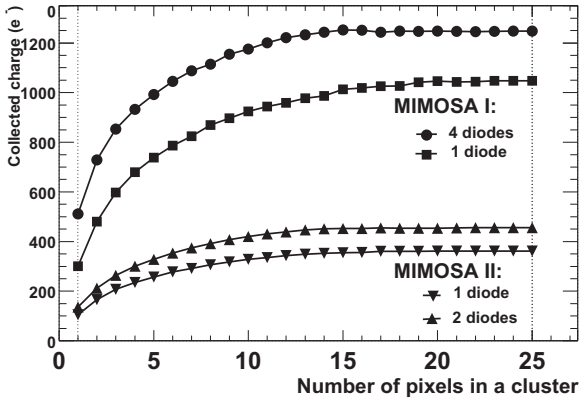

Figure 6-38: Collected charge (most probable value) as a function of the cluster size.

6.8.2 Signal-to-Noise Ratio

Figure 6-39 displays the SNR for the central pixel of a cluster for minimum ionising particles for MIMOSA I. The central pixel was identified by requesting an individual signal to

noise ratio above five and taking the pixel with the highest SNR value within a cluster of neighbouring pixels. The variation of the clusters SNR with their size was measured to exhibit better performances for the single-diode pixel configuration.

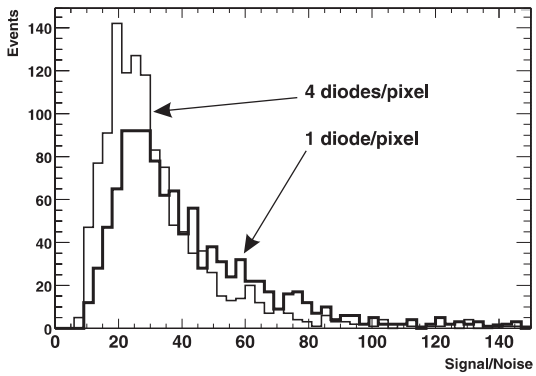

Figure 6-39: Signal-to-noise distribution for the central pixel in the reconstitued cluster in the MIMOSA I chip.

The mean value of the SNR reaches 42 in this case, while for the four-diode pixel configuration it was 32. In the case of MIMOSA II, the mean value of the SNR was 21 and 18 for the single diode and two diode pixel configurations, respectively. The cluster noise was taken here as the average single-pixel noise times the square root of the cluster multiplicity.

6.8.3 Tracking Performance

Tracks of particles were reconstructed in the telescope by requiring at least on hit per plane and by adjusting a straight line to the eight telescope co-ordinates. After internal alignment, the intersection of the tracks with the MIMOSA sensor plane was known within approximately 1 μm precision. The intersections were compared to the results of an independent cluster finding procedure applied to the sensor data. The cut of five was used for SNR for the seed pixel finding procedure.

Several thousand tracks reconstructed in the telescope were interpolated within the geometrical acceptance of the sensor. For almost all of them, a cluster was found in the sensor in the vicinity of the interpolated point, i.e. within a few tens of micrometers, usually between 20 μm and 30 μm. This translated into a preliminary value of the detection efficiency of 99.5%±0.2%, 99.2%±0.2%, 98.5%±0.3% for the single and four diode pixel configurations in MIMOSA I and the single diode pixel configuration in MIMOSA II, respectively.

In order to determine the pixel detectors spatial resolution, the track parameters extracted from the reference beam telescope were compared to the positions extracted from the pixel device using two different methods. In the first method aiming at so-called binary resolution, the track position was given by the centre of the pixel exhibiting the highest SNR in the cluster. In the second method (CoG), the track position was taken as the centre of gravity of the charge within a 3 × 3 pixel cluster. Using the second method for the single diode pixel configuration in MIMOSA I, a gaussian fit to the residuals of the reconstructed and extrapolated track positions gave a standard deviation of 2.2 μm. This result could still be improved using a non-linear correction to the CoG algorithm. The s-shaped correction function was derived from the correlation between the track position given by the reference telescope and the position given by the pixel sensor data using the CoG method. Figure 6-40 shows the corresponding plot of correlation between the track positions given by the reference telescope and by the pixel sensor data using the centre of gravity of a 3 × 3 pixel cluster for the single diode pixel configuration in MIMOSA I.

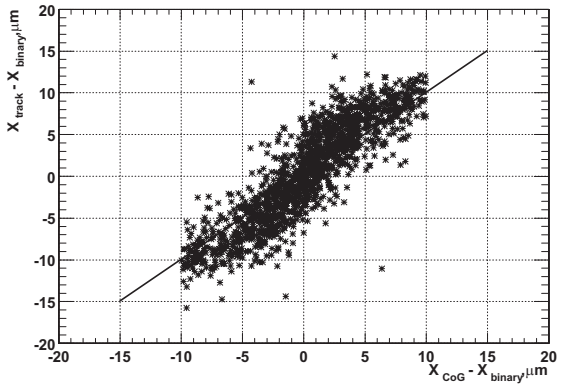

Figure 6-40: Correlation between the track positions given by the reference telescope and by the pixel sensor data using the centre of gravity of a 3 × 3 pixel cluster for the single diode configuration in MIMOSA I.

The width of the residual distribution varied slightly as it was calculated for data taken at different runs. After the correction with the s-shape function the best value of the standard deviation of the residual was found to be 1.72 μm. The spatial resolution was calculated by performing a gaussian fit to the obtained distributions. Taking into account the estimated precision of the telescope (1 μm), the spatial resolution of the single diode pixel configuration from MIMOSA I based on the centre of gravity position determination

algorithm was estimated to be 1.4 μm±0.1 μm in both directions. The best resolution was achieved with the single diode pixel configuration in MIMOSA I, since the charge distribution was widest and the SNR was the highest in this case. Following the same algorithm for other pixel configurations and the second prototype, the spatial resolution was estimated to 2.1 μm and 2.2 μm for four in MIMOSA I and the single diode pixel configurations in MIMOSA II, respectively. Figure 6-41 shows residual distributions of a track position measured by the single pixel configuration in the MIMOSA I chip for two different algorithms used, i.e. binary resolution, and CoG with the non linear correction, compared to, the MIMOSA II chip treated with the CoG method. Figure 6-42 shows the two-dimensional distribution of the distance between the track position at the plane of the MIMOSA chip under test measured by the reference telescope, and the one reconstructed for all clusters by the MIMOSA I sensor itself. It is noticeable in Figure 6-42 that for most of the tracks, a cluster was found within a distance of 20 μm. Some hit position identified outside the main peak were considered as a statistical relevant in the data analysis.

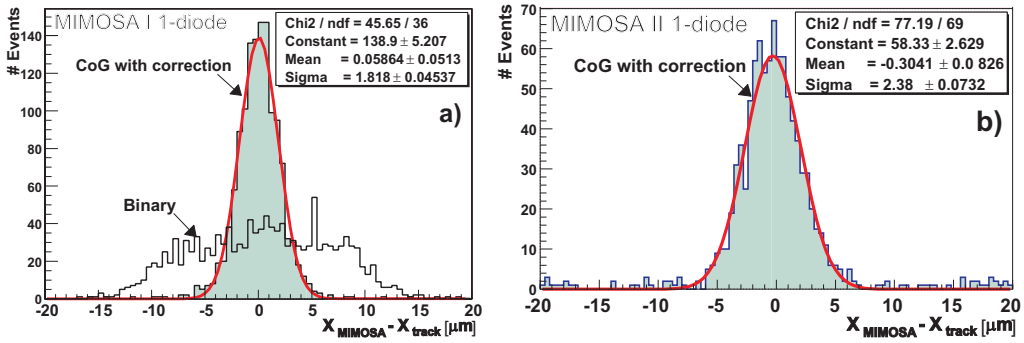

Figure 6-41: Residual distribution of a track position measured by the (a) single diode pixel in the MIMOSA I chip for binary and CoG methods, (b) related distribution for the single diode pixel configuration in the MIMOSA II chip for CoG.

The chip sensitivity to temperature was tested with the MIMOSA II chip, which was successfully tested at room temperature with a read-out frequency of 10 MHz. No degradation of the performance, including SNR and the spatial resolution, was observed in the increasing temperature interval from –10°C to 20°C.

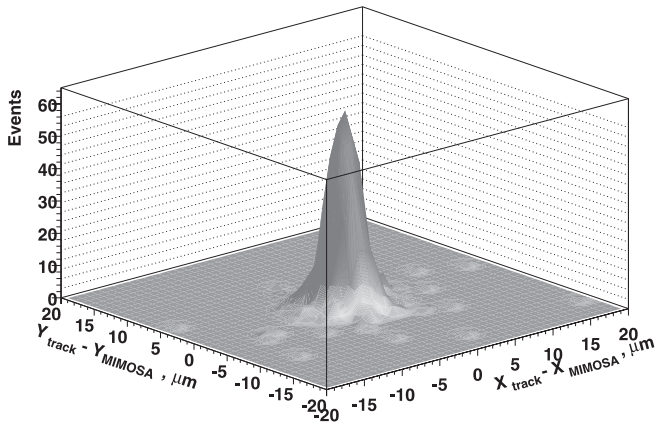

Figure 6-42: Two-dimensional position distribution of all reconstructed clusters with respect to the reference tracks.

6.9 Influence of Strong Magnetic Field on Charge Collection

The possibility to operate the MIMOSA chips in high magnetic fields was investigated with an X-ray source at the superconducting magnet "JUMBO" at the Institut für Experimentelle Kernphysik, Universität Karlsruhe, Germany. The magnet is capable to produce a magnetic field of up to 10 T in a small volume approximately $10 \times 10 \times 10$ cm^3. The superconducting coil consists of niob-titatium (NbTi) and is cooled by liquid helium during operation.

The measurements were possible at temperatures going up to the room temperature, because the detector and the excitation source were located within an isolated tube reaching down into the magnet. The magnetic field dependence of the total charge generated by X-ray photons from a ^{55}Fe source and collected in MIMOSA I for different field orientations and strengths was studied. Two orientation of the magnetic field with respect to the detector surface were examined, i.e. the detector surface was initially aligned parallel and then orthogonal to the direction of the magnetic field. For each orientation of the magnetic field five strengths were used (0 T, 1 T, 2 T, 4 T and 6 T), and a few thousand events were acquired. The results of this spectroscopic approach are shown in Figure 6-43 for two orientation of the magnetic field. Results of theses tests demonstrate that fields going up to 6 T have only a modest influence on the cluster shape and charge collection. Thus, graphs shown in Figure 6-43 include only extreme cases, i.e. with magnetic field amounting correspondingly to 0 T and 6 T. It is noticeable in this figure that the position

of the second peak, determining the conversion gain, remains unchanged regardless the strength and orientation of the magnetic field. It follows that the charge-to-voltage conversion gain of the pixel is not affected by the magnetic field.

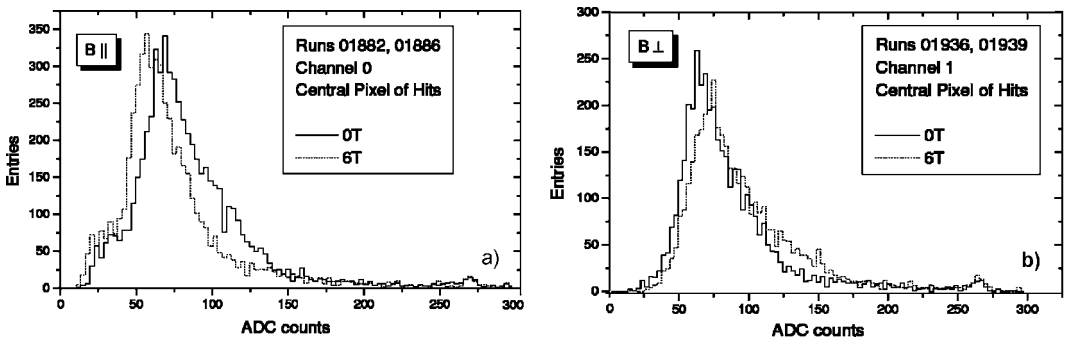

Figure 6-43: Central pixel histogram in the MIMOSA I sensor for the magnetic field (a) parallel and (b) perpendicular to the surface of the sensor.

But, it can clearly be seen that the "big" peak resulting from photons converting within the bulk of the MIMOSA I chip slightly moves with increasing magnetic field, shifting towards lower and correspondingly higher ADC counts for parallel and orthogonal magnetic field orientations with respect to the detector surface. This means that the average amount of the collected charge varies with magnetic field. The parallel orientation of the magnetic field translates to less charge collected by the central pixel, while the effect of the orthogonal field is opposite. The same effect as for the central pixel was observed for the 3×3 pixels cluster, where most of the generated charge is collected. Table 6-16 summarises results on the magnitude of the signal peak shift for the 3×3 pixels cluster in the case of the MIMOSA I chip oriented in the parallel and perpendicular way with respect to the external magnetic field.

Table 6-16: Magnitude of the signal peak shift for the 3×3 pixels cluster in the case of the MIMOSA I chip in the external magnetic field.

	Shift of signal peak				
Test conditions \ Magnetic field	**0 T**	**1 T**	**2 T**	**4 T**	**6 T**
MIMOSA I B ‖	0%	<-1%	-2.0%	-5.6%	-9.4%
MIMOSA I B ⊥	0%	n.a.	2.5%	5.8%	7.0%

The shift of the signal peak does not exceed 10% of the initial peak position and other detector parameters including the charge-to-voltage conversion gain are unaffected. Thus, the influence of the strong magnetic field on the detector performance is evaluated as very modest.

Chapter 7

PERSPECTIVES AND FUTURE WORK

7.1 Further Development and Improvement of MAPS Performances

First results obtained with small-scale MAPS prototypes, representatives of a novel technique for silicon position sensitive detectors, are very promising. The technology has been proven its capability for minimum ionising particle detection. Several requirements for a vertex detector at TESLA are already fulfilled. This makes the MAPS technology a good choice for a vertex detector construction in competition with CCDs and Hybrid Pixel Detectors. The related R&D programme towards the development of this technology has already been officially approved by the DESY Physics Research Programme Committee [109]. The good parameters deduced from results achieved with small MIMOSA chips still need to be ascertained with a real size detector fabricated from the prototype designs. Several other requirements are still to be met, most of which were outside of the scope of the work done hitherto. This part of work consisted primarily of demonstrating that the sensor technology was adequate for charged particle detection. In particular, further development is required on the charge sensitive element, the front-end electronics, and the architecture allowing increasing read-out speed, data sparsification and optimisation of power consumption. Those were not a major concern for the first step of development. The established intrinsic performances of the sensor technology are likely to be subject of improvement, since the technology potential is still far from being fully explored. Such investigations aim at, among other, further reducing the electronic noise, improving the charge collection efficiency, adapting charge sensitive elements to the specific conditions of the foreseen applications, implementing on-line and on-chip signal processing capabilities, i.e. to move the most critical part of analogue processing on the pixel level, exploring various manufacturing processes, finding the optimal operation conditions in terms of temperature, SNR, read-out speed, etc. The aim will be to read-out a ladder; a row of chips with several million of pixels, in time interval of the order of 50 μs – 100 μs or less by subdividing the

array into sub-matrices read out in parallel. Preliminary results show that the radiation tolerance of the sensors, in particular to neutron radiation, already seems sufficient for the future Linear Collider. The observed sensitivity needs to be understood and iterations will be required to improve the radiation resistance well beyond the present limits, in particular for ionising radiation.

The ongoing optimisation towards the final read-out architecture of the MAPS detector will be propagated to the design of the data acquisition system developed in parallel. The main issue is the potentially large amount of data due to beam-induced background.

Whether the ladders can be fabricated at the desired size or whether chips as large as a CMOS reticule, which is approximately 2×2 cm^2, need to be assembled to form a ladder, is an open question. In order to go towards larger sensor areas, two options are considered, i.e. the "clever dicing" and stitching option. In the "clever dicing" option, sensors are designed to cover the full reticule. For a 20-μm pitch device, one of those sensors would typically have about one million pixels. The design of the sensors is such that minimal dead areas are kept along the side of the pixel matrices. Typically, silicon technology requires dead areas of less than 100 μm. At the dicing operation, units of 6 – 7 reticules are kept together so to form a ladder. The mentioned dead space is perfectly tolerable in most of the cases. This technique will neither introduce any feature harming the circuitry design or any of the sensor performances. In the stitching option, which is now more and more often proposed by foundries, sensors of the required size are designed with no dead space. Thus, wafer size sensors are becoming a real possibility, and the parallel column-wise data handling with data processing directly on a chip, including efficient on-line data sparsification is a recipe for a successful design of a vertex detector. The parallel column-wise data handling is actually essential for achieving a high read-out speed. In the MAPS design, in contrast to CCDs, the signals can be read out along columns parallel to the shortest dimension of a ladder, i.e. transversely to the beam lines, which allows maximal parallelism in data treatment. The latter may be achieved with data processing circuits, potentially including simple signal discriminators or a few bit precision analogue-to-digital converters, integrated on a narrow band of the ladder. The space occupied by the read-out circuitry should be kept below 10% of the active detector area in order to maintain its consequences on the material budget at an almost negligible level. In the cylindrical construction of a vertex detector, small excess part

of each detector ladder overlaid another ladder is necessary to avoid presence of blind angle.

In the design of MAPS detectors, power dissipation has to be minimised. It should be kept within a range demanding moderate cooling only, detectors can be operated as a matter of fact close to room temperature. Additionally, the thinning of sensors down to the limits set by their mechanical properties also needs to be investigated since the desired thickness of typically 50 μm is not a straightforward operation, nor is the handling and mounting of very thin sensors.

The following sections address the design work which has already been commenced after the first successful small scale prototypes. The description of the first large, wafer-scale prototype called MIMOSA V, which has been designed and received recently from fabrication*, is provided. Then, two new ideas for improving the conventional photodiode-type design with proposition for the associated pixel-level read-out circuitry are presented. The novel two-diode logarithmic pixel design and current mode pixel called photoFET, while the latter features signal amplification capability built into the charge sensitive element, are proposed. Based on the two-diode scheme for self-reverse biasing of the charge collecting diode, the first attempt for implementing analogue signal processing directly on the pixel level has been developed. The MAPS sensor with on-pixel amplification and double sampling operation has been implemented on the next small-scale prototype MIMOSA VI chip submitted for fabrication in a 0.35 μm CMOS process. Perspectives for different fabrication processes, which can potentially be used for MAPS detectors, are also provided.

Whilst the active element may vary, the principle of using the moderately doped epitaxial layer or so called high resistivity wafers for fabrication of integrated circuits for 100% fill factor and a very good detection efficiency at room temperature seems essential. All approaches to improve sensor performances require extensive simulation, prototyping and test programmes.

7.2 Wafer Scale MAPS Detector Ladder

In order to apply MAPS detector technology for a vertex detector in any high-energy physics experiment, the performances obtained with small MIMOSA prototypes need to be

* The MIMOSA V chip has been received from fabrication in March 2002.

reproduced with a large-scale device of the whole wafer surface. The first circuit designed with the intention to answer the question if any detector parameter, like noise performance, charged particle tracking efficiency and radiation hardness, deteriorates with the increasing scale of the device is the MIMOSA V chip. The device, whose schematic layout is shown in Figure 7-1, has been designed using pixel configurations based on the MIMOSA I design and the read-out architecture has been altered to be compatible with large geometrical dimensions of the chip and large number of active elements. Furthermore the MIMOSA V prototype is foreseen to investigate directions, which were for practical reasons out of the scope of small prototypes. This includes yield studies as well as testing device-thinning procedures[*,†].

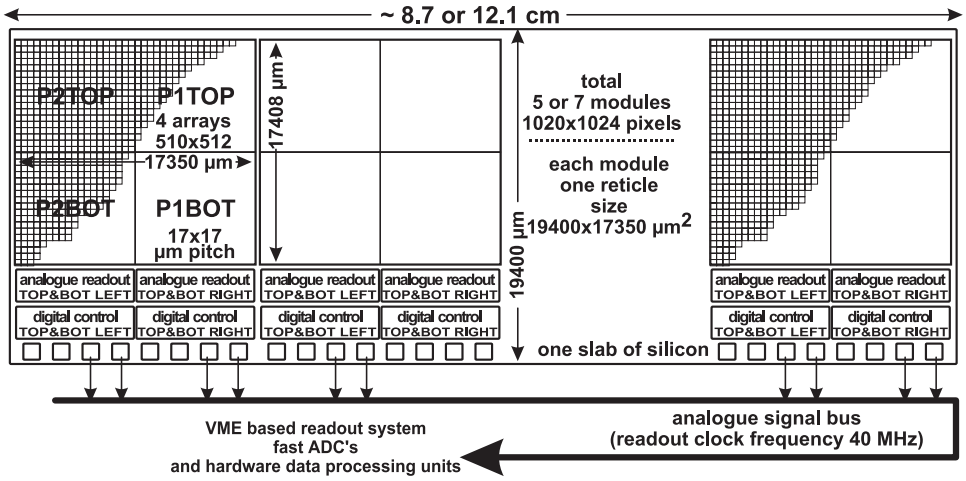

Figure 7-1: Schematic layout of the detector ladder with the MIMOSA V prototype.

First wafer scale MAPS prototype MIMOSA V has been designed and manufactured using a 0.6 µm CMOS process. Its basic unit is a one reticule size (19400 × 17350 µm^2) chip made of four arrays of 510 × 512 active pixels, i.e. in total 10^6 pixel device, laid down with a an uniform pitch of 17 µm in both direction. Each constituent chip is equipped in four independent parallel analogue outputs, i.e. one output per each array. The read-out electronics chain and noise performance have been optimised to achieve maximum read-out clock frequency, determining pixel read-out rate, of 40 MHz. The basic modules are aligned

[*] The detector to be applicable for a vertex detector construction in future linear collider experiment needs to be thinned down to the thickness in the order of 50 µm.

[†] At the current stage the MIMOSA V chip is not scheduled to respond quanitatively to requirements of a collider experiment, e.g. TESLA, in terms of timing for read-out and data transfer.

together in one direction on the wafer using the "clever dicing" option. In this option, there is no electrical connection provided between modules. The structure is repeated five and seven times on the 6" wafer, with an interface band of the dead area in-between of approximately 200 μm. This results in of 8.7 cm or 12.1 cm long detector slabs. The read-out electronics is placed at the bottom of each unit, occupying a band of approximately 2 mm width, including input/output pads. All bonding pads and read-out control logic cells are grouped along one edge. The photograph of a wafer with MIMOSA V prototype before lapping and cutting is shown in Figure 6-2, where the right hand side picture is a zoomed view showing details of the basic modules abutted in one direction and with bonding pads occupying only one side of the ladder.

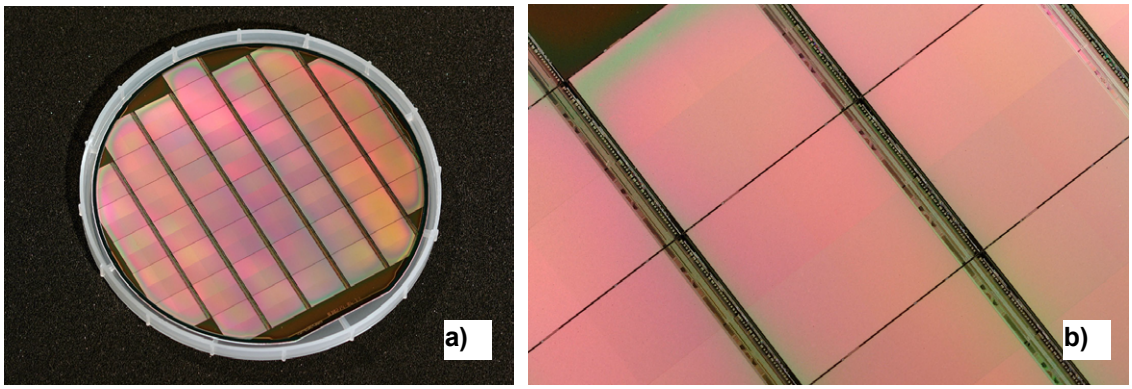

Figure 7-2: (a) Picture of a wafer with MIMOSA V prototype before lapping and cutting, (b) detail of the MIMOSA V wafer.

The chip was equipped with several read-out options, which are supplementary to the standard MIMOSA I like operation. The basic read-out option is similar to the MIMOSA II chip with pixels being addressed sequentially one after another to be read-out and several read-out lines multiplexed onto one output buffer. In the MIMOSA V chip, long read-out lines exhibit parasitic stray capacitance of approximately 8 pF and less than 4 pF, for vertical and horizontal readout lines, respectively. Due to the presence of these large capacitances, double buffering of analogue signals has been used. Source followers with PMOS transistors have been added at the bottom of each column. The outputs of PMOS source followers are connected to the horizontal read-out lines via analogue transfer gates driven from column selection digital signals *COL_SEL*. There are six horizontal read-out lines. *COL_SEL* lines are also used to turn on currents into column read-out lines biasing source followers in pixels selected for being read out.

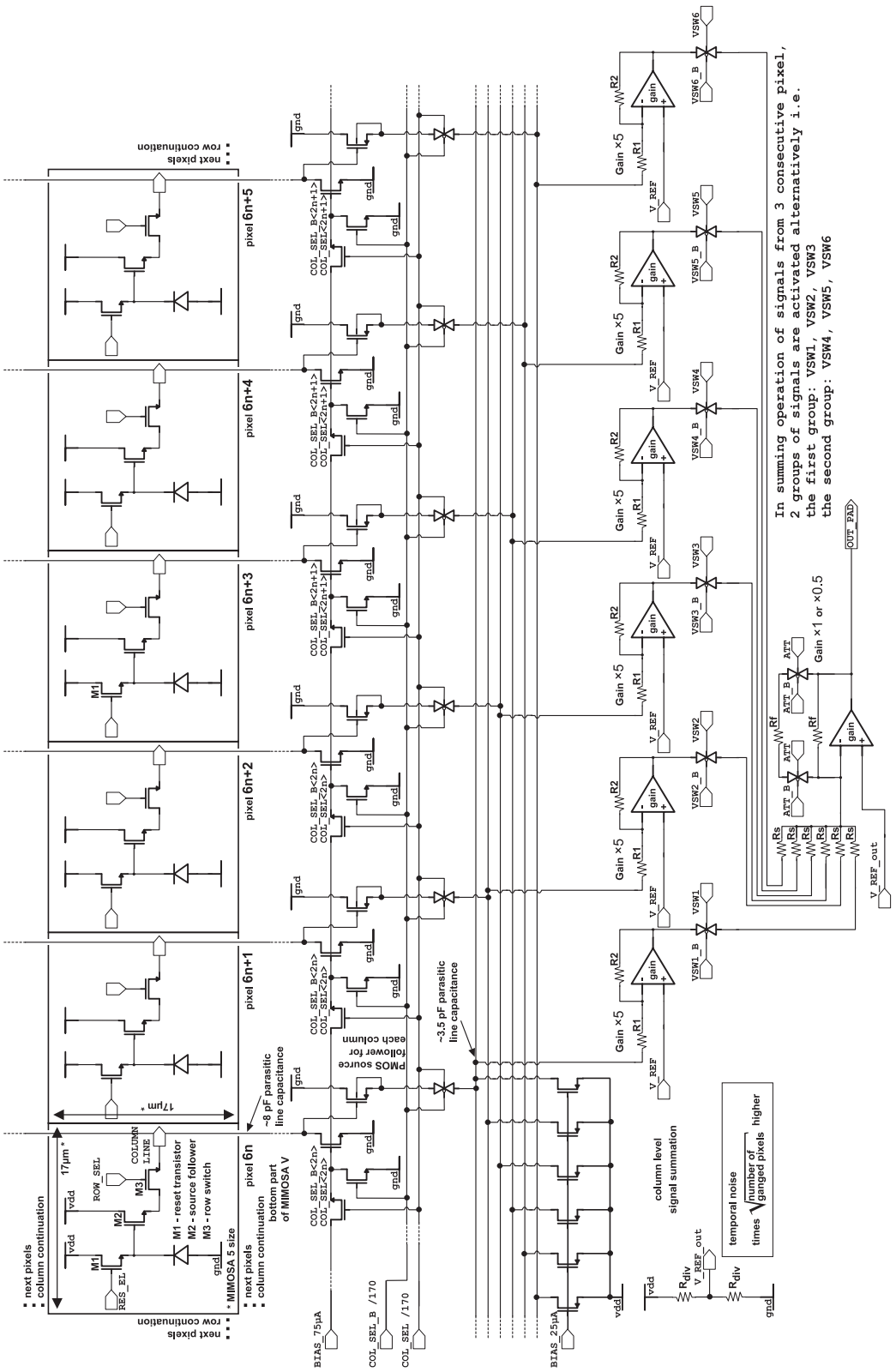

Figure 7-3: Principle of MIMOSA V operation with signal summation from three contiguous pixels and other readout options.

In order to provide fast settling time of signals, the bias current in the pixel source follower is increased to 75 μA with respect to typical bias current in previous MIMOSA chips in the range of 10 μA to 25 μA. The nominal bias current in PMOS source followers is 25 μA. Each of six horizontal read-out lines is terminated with a voltage amplifier providing a gain of 4. Outputs of this amplification stages are multiplexed on to the output buffer, which can provide a gain of unity or half. The gain value is selected by an external digital signal *ATT*. The output buffer can be configured as a stage performing summation of signals from horizontal lines. For the total number of 510 columns of pixels in the array, only 170 distinct *COL_SEL* signals are present. This implies addressing of columns in triplets from contiguous vertical lines. In the basic operation mode, only one *VSWXX* signal is active, thus only one column is multiplexed at once onto the read-out buffer. Addressing of columns in triplets determines the time interval in which a given column is being "prepared"* to be read-out, while another column is being read-out. This interval varies between three to five read-out clock cycles for the first and the last column in the addressed triplet, respectively. The chip read-out can be reconfigured to the mode, allowing scanning the array in a fast selective mode, where only each third pixel is read out. This mode is achieved by reducing the duration of the *COL_SEL* signal to only one read-out clock period, dividing by three the duration of the row selecting signal *ROW_SEL* and activating only *VSW1* and *VSW4* signals. The effective read-out pitch in the direction of rows can be increased to $3 \times 17\ \mu m = 51\ \mu m$ by performing summation of analogue voltage signals from pixels forming a triplet. In both read-out modes, the time interval throughout which the signals settle down before reading out is reduced to one period of the read-out clock. The half gain of the output buffer is provided to be used in this mode; since summed signals may exhibit relatively high pixel-to-pixel offsets and resulting signals can saturate the output buffer. An additional option implemented on the chip is the rolling reset capability, in which each row is reset immediately after all pixels from this row are already read out. The detailed schematic diagram of the MIMOSA V chip topology is shown in Figure 7-3. The reference voltage for the six first stage amplifiers is provided externally, while the reference voltage for the output buffer is set to the half of the power supply voltage by the use of simple resistance divider. The MIMOSA V chip has been designed non-conforming to the layout rules for increasing

* The detailed descriptio of this read-out mode using two phase signal preparation is provided in Chapter 5.2.

radiation hardness. All transistors, except the reset transistor in a pixel, are designed with a standard rectangular form of a polysilicon gate. The serial analogue output of the chip will be connected to the new version of the VME based data acquisition system equipped with a sufficiently large amount of memory for storing information from a few millions of pixel and an on-line data processing unit for CDS processing, pedestal suppression, noise analysis and potential selection of hit pixels.

The decision to read a detector ladder "sideways" rather than along the ladder length* can be advantageous in the case of MAPS, because it allows to localise signal processing electronics closer to the sensor and transfer to the data acquisition system only processed and selected information along the ladder length. Such detector design is possible because of natural integration capability of the detector with the read-out electronics on the same substrate resulting from the use of a CMOS process. Shorter control lines allow easier distribution of clock and control signals. These signals distributed to pixels can be generated from one common to all units clock line. Subdividing the detector ladder in relatively small blocks processing analogue data in parallel would potentially allow to use lower clock frequency to access pixels than is required in the case of detector read-out along the ladder length. Implementing random access to pixel can increase performance of the read-out electronics placed at the bottom of each sub-array. This approach can fully prove its efficiency in combination with continuous search for presence of physical signal within any sub-array area. In order to provide this capability, special low-noise pixel electronics, like this presented in Chapter 7.3.2, is needed.

7.3 Alternative Charge Sensitive Elements and Pixel Designs

The design of alternative charge sensitive elements presented in this chapter, in view of the required 100% charge collection efficiency, includes only modifications of the n-well/p-substrate diode collecting the charge generated by a charged particle traversing the detector medium. The work was oriented on introducing the possibility of a continuous reverse bias on the charge-collecting element, which would suppress the effect of a voltage drop due to

* The read-out along the detector ladder is proposed as a single option for CCDs. The "sideways" option is not achievable for CCDs technology, since it does not allow to integrate electronics with the detector onto the same surface. For CCDs, columns along the ladder are read out in parallel to decrease sensitivity to radiation bulk damage.

the leakage current, and implementing signal amplification in the charge sensitive element. A constant continuous bias allows implementing on-pixel signal amplification providing a good SNR value as an essential requirement to realize the equivalent of a correlated double sampling operation on the pixel. The presence of leakage currents varying significantly from one pixel to another, makes it impossible to implement signal amplification in either DC or AC –coupled configuration, because the identical nature of leakage current and physical signal. Such a situation is shown in Figure 7-4, where the physical signal is over imposed on the slope resulting from the leakage current.

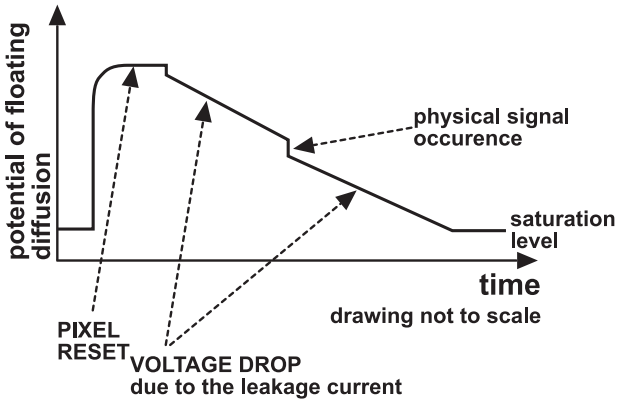

Figure 7-4: Potential drop on charge sensitive element caused by leakage current with physical signal superimposed on the slope.

Application of other charge sensitive elements, e.g. a photogate that is commonly used in visible light detection [110, 111], was not studied in the framework of this thesis. They seemed less applicable to charged particle detection or their design was not straightforward in a standard CMOS technology. In the case of the aforementioned photogate element, a direct access from the detector surface to the epitaxial layer is required. Most fabrication processes feature complementary twin-well option. The designer, drawing an n-well area, defines the remaining part of the chip to be filled with a p-well. The presence of the p-well is considered as an important obstacle for collecting charge carriers from the interior region constituting an active detector volume. Only very few processes, intrinsically those offering a native (V_{TH}=0 V) NMOS transistors, offer the opportunity to have direct access from the chip surface to the layer of low doping level.

7.3.1 Two-Diode Design for Self-Reverse Bias of Charge Sensitive Element

7.3.1.1 Charge Sensitive Element

The classical pixel structure with three MOS transistor cell and an n-well/p-epi diode used as a charge-collecting element operates in a linear mode. The charge collected ensues voltage response of the pixel via the source follower transistor. The charge-to-voltage conversion gain for this structure, neglecting any second order effects, is independent of the signal magnitude. Pixel detectors functioning in linear mode are characterised by charge integration taking place throughout the exposition time and than the charge contents of a pixel needs to be cleared to the initial value. This is achieved by the reset operation periodically performed on the charge-collecting element. In particular applications for detection of visible light, the use of pixels operated in the linear mode suffers from some limitations. The limitations firstly consist in the presence of blooming effects in exposures to scenes characterised by very large differences of light intensities, and secondly the random, continuous access to the sub-images in the whole frame is excluded. This is because of the requirement to synchronise the read-out operation with the charge integration period. Pixel devices operated in a non-linear, logarithmic mode meet the requirements, which are complementary to the linear mode devices. Logarithmic response pixels do not integrate the charge, but a logarithmic relation approximates their voltage response V to a light instantaneous power P: $V = A \cdot \mathbf{log}\, P$. The logarithmic pixel characteristic can be interpreted as an intrinsic signal compression capability. It translates the wide dynamic range of the pixel response, typically up to six decades of light intensity, to constant image contrast and gives the possibility of random access to pixels during all the exposition time.

The conventional method to obtain a logarithmic pixel response consists in the use of a MOS transistor in the diode configuration as a load of a photosite element [112, 113]. Logarithmic response of a pixel is obtained thanks to the exponential dependence of the transistor drain-source current on its gate-source voltage. Pixels operated in the logarithmic mode can be arranged in a two-dimensional array using the same circuitry as it is realised for their linear response counterparts, i.e. using a simple source follower stage of close to unity voltage gain for adapting an output impedance, and a system of switches for pixel addressing. Logarithmic conversion transfer function of the incident light intensity into the voltage signal

can also be achieved using a junction diode as a load of the charge collecting diode as it is shown in Figure 7-5a. The loading diode can be realised in a standard CMOS process by implanting a shallow p^+-type region into the n-well. The similar structure was formerly proposed for a double junction photodiode allowing for selective light detection of different wavelengths [114]. The whole structure here proposed consists of a deep n-well implanted in a moderately doped p-type substrate region, which is usually in a form of an epitaxial layer, and two shallow regions of increased doping levels implanted in the n-well. The first region of the n^+-type doping is used to form a contact allowing to connect the charge-sensing element to the read-out circuitry. While, a p^+-n junction is formed by the second region of the p^+-type doping region placed in the n-well. Application of the positive potential on the p^+-type region, with respect to the substrate, provides a slight forward bias of the junction. The two-diode structure is obtained, where the diode D1 collecting the charge carriers is reverse biased and the load diode D2 is polarised in forward direction. In darkness, the diode D2 conveys only a small value leakage current, and represents an equivalent resistance typically in the order of $10^9\ \Omega - 10^{12}\ \Omega$. The resistance realised in this way is non-linear and decreases with increasing height of signals. Under the presence of a strong physical signal or under high illumination conditions the collected charge by the diode D1 is drained by the diode D2, constituting its conduction current. The electric potential of the n-well, as a logarithmic function of the current is accessible for read-out through the n^+-type region. For visible light applications the new solution offers simplification and compactness of the pixel design. The pixel size can be reduced and the quantum efficiency increased. These effects are achieved by diminution of metal connections and number of corresponding contacts within the pixel area.

On the other hand, the charge integration capability of the two-diode structure proposed is assured for detector operated under environment of low signal intensities and low individual signal amplitudes. The signal level must be in the range, for which the decay time constant, defined by the equivalent resistance of the forward biased diode and the capacitance of the n-well, remains much longer than the time interval between two detector read-out cycles. A vertex detector designed for particle physics experiments is a device operating in darkness. It experiences only sporadic hits due to particles traversing the medium. Under these conditions, the ultimately high resistance of the load diode can be used

to design a new charge sensitive element for charged particle detection. The new structure of the two-diode for charged particle detection is here proposed. The view of the structure is shown in Figure 7-5b. This is compatible with a standard CMOS process used for design of MAPS devices. A continuous reverse bias of the charge collecting diode is provided and the high resistance of the loading diode allows charge integration with a very long decay time constant. In order to validate the proposed idea, already one array of pixels in the MIMOSA IV prototype was for the first time equipped with two-diode pixels.

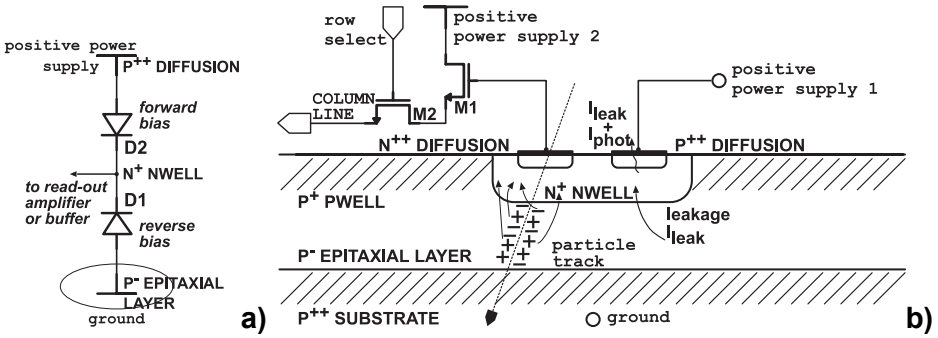

Figure 7-5: Two-diode logarithmic pixel, (a) principle of continuous reverse biasing, (b) conceptual design of pixel structure exploiting continuous reverse bias of the diode for charge collection.

The read-out circuitry in this test structure was very simple, based on the classical solution with a source follower stage placed in each pixel. The test structure from the MIMOSA IV chip was tested with sources of visible light to evaluate the sensitivity of the device, and a high-energy charged particle beam to estimate the adequacy of this new pixel architecture to charged particle detection.

7.3.1.2 Tests with Visible Light Sources

The measured response of the two-diode logarithmic pixel to light emitting diode sources of different wavelengths is shown in Figure 7-8. The HLMP-4101, HLMP-CM15 and HLMP-CB15 diodes were used, which are emitters of light of wavelengths of 626 nm (red), 524 nm (green) and 470 nm (blue), respectively [115]. During the test, the device was continuously illuminated with light of a varied intensity, and the pixel response was measured as the output voltage level corresponding to each illumination. The measurements of power of the emitted light require generally the use of calibrated photo-detectors. However, the intensity of the emitted light by the LED diode and the bias current of this element are proportional. The

linear relation between them is satisfied in a very good approximation for a wide range of currents. Thus, instead of measuring directly the emitted light power, the LED diode current was referred to as the measure of the light intensity. The pixel responses obtained show the dynamic range of more than five decades of the diode current for each light wavelength.

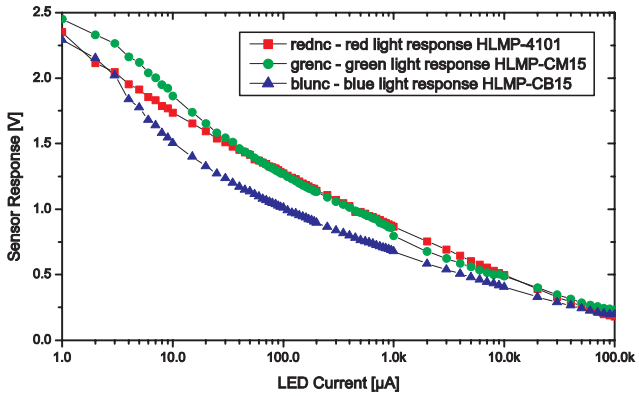

Figure 7-6: Response of the two-diode logarithmic pixel to LED diode sources of different wavelengths RGB (626 nm, 524 nm, 470 nm).

The measurements, performed with sources of visible light, allowed validating the proposed pixel structure as a detector element characterised by logarithmic form of its transfer function.

7.3.1.3 Tests with a Charged Particle Beam

The usefulness of the two-diode pixel design for charged particle detection was verified in tests performed with a high-energy particle beam of 120 GeV/c pions from the SPS accelerator at CERN. During the beam-tests, the typical configuration of the test set-up with the MIMOSA chip sited in the middle of the high precision beam telescope with scintillating counters delivering trigger signal was used. The detailed description of the beam test set-up and the methodology of the data analysis is provided in Chapter 6.2. The preliminary results of data analysis are very promising. The tracking performances of the new pixel structure does not depart from those obtained for other MIMOSA chips featuring a standard three MOS pixel configuration. The measured response of the two-diode logarithmic pixel to the charged particle beam is shown in Figure 7-7. The left side plot in this figure displays the signal-to-noise ratio for the central pixel of a cluster. The central pixel was identified by requesting an individual signal to noise ratio above five and taking the pixel with the highest

signal value within a cluster of neighbouring pixels. While, the right side plot shows variation of the amount of the collected charge as a function of the cluster size. Pixels were successively added to form a cluster in decreasing order of their signal amplitudes. The charge spread appears to be much wider in the case of the MIMOSA IV chip with respect to the MIMOSA I or II devices.

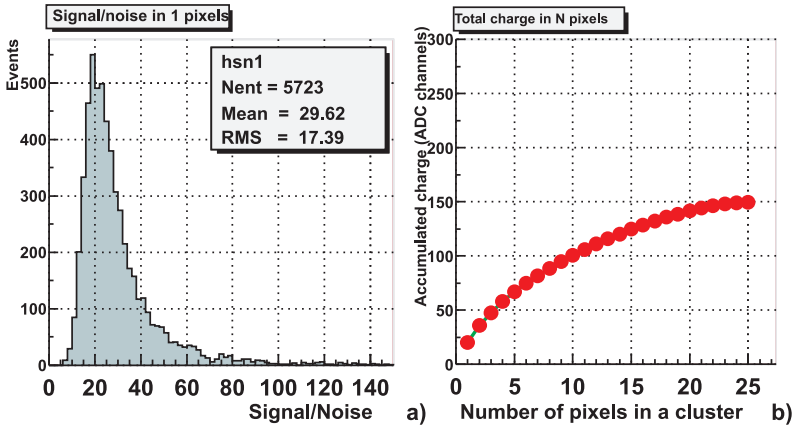

Figure 7-7: Response of the two-diode logarithmic pixel exposed to the charged particle beam; (a) signal-to-noise ratio for the central pixel, (b) collected charge (most probable value) expressed in ADC units as a function of the cluster size.

This wider charge spread observed in Figure 7-7 occurs over about 25 pixels per cluster, due to the use of non-epitaxial substrate of increased resistivity for device fabrication, with respect to the standard wafer substrate. The accumulated charge in the right side plot has been expressed in ADC units before calibration of the charge conversion gain for the charge sensitive element in the chip tested, and the signal is referred as to the most probable value of the Landau-like distributions obtained for different cluster multiplicities. The mean value of the signal-to-noise ratio reaches approximately 30 in the case of the self-reverse bias pixel configuration from the MIMOSA IV chip. The cluster noise was taken here as the average single-pixel noise times the square root of the cluster multiplicity. The tests showed equally the usefulness of the new pixel structure for applications consisting in charged particle detection and tracking.

7.3.1.4 Design of the Pixel with on-Pixel Signal Amplification and Double Sampling Operation

Following the first promising tests with a two-diode logarithmic pixel configuration for

charged particle detection, a completely new full design of the pixel is proposed. The development of the new pixel concept is considered as a part of the research work aiming to fulfil highly demanding performances of the vertex detector foreseen at the future linear collider. The final vertex detector design will necessitate implementation of the on–chip processing with efficiently performed on-line data sparsification. Achieving high read-out speed will require parallelism in the performed operations and compression of the flow of the data transferred to the acquisition system. The proposition of the new pixel concept is considered as a first step to implementation of signal processing functionalities, including data sparsification, performed on-line on the detector. The pixel design proposed exploits the continuous reverse biasing capability of the charge collecting diode, which makes the design of the on-pixel signal amplifier feasible.

The new approach to design a detector basing on the MAPS detection concept combines on-pixel signal amplification and double sampling read-out operation. It provides an output signal resulting from the difference between the charges collected in two consecutive time slots. Efficient signal discrimination with high SNR provided requires signal amplification with the gain as a rule of thumb in the order of $5-10$ and suppression of pixel-to-pixel non-uniformities. The continuous bias eliminates voltage level drop due to accumulation of charge carriers resulting from the leakage current of the charge sensitive element. In this case, a stage providing a reasonable signal gain can be driven from the charge-collecting element without any concern for the dynamic range.

Schematic and timing diagrams of the proposed pixel design are shown in Figure 7-8. The pixel design has been implemented for testing purposes on the MIMOSA VI chip, which has been recently submitted for fabrication*. The pixel design is foreseen to match with a signal discriminating stage, which was also designed and implemented on this chip†. The design originates from a classical MAPS design, and as the previous scheme, it can be fabricated in standard CMOS fabrication process. The new pixel design uses only NMOS transistors, n-well/p-epi and p-diff/n-well diodes and poly1-to-poly2 linear capacitors. It is based on a principle of switched operation of the circuit with 15 transistor switches close to

* The MIMOSA VI chip has been submitted for fabrication in the Alcatel Mietec 0.35 μm CMOS process at the fabrication run on April 2002.

† The design of discriminators was done by the group from Commissariat à l'Energie Atomique (CEA) in France in the frame of the formed collaboration.

minimum size, allowed in the process used, and 14 transistors used for the active signal amplification. The amplifier is operated in a switched power consumption mode. The total power consumption during the read-out phase amounts to 316 μW at 3.3 V of the power supply, while for the remaining time the power consumption is negligible. The design permits performing double sampling on a time interval of the frame-rate, and the output signal from the pixel corresponds to the difference of two samples acquired.

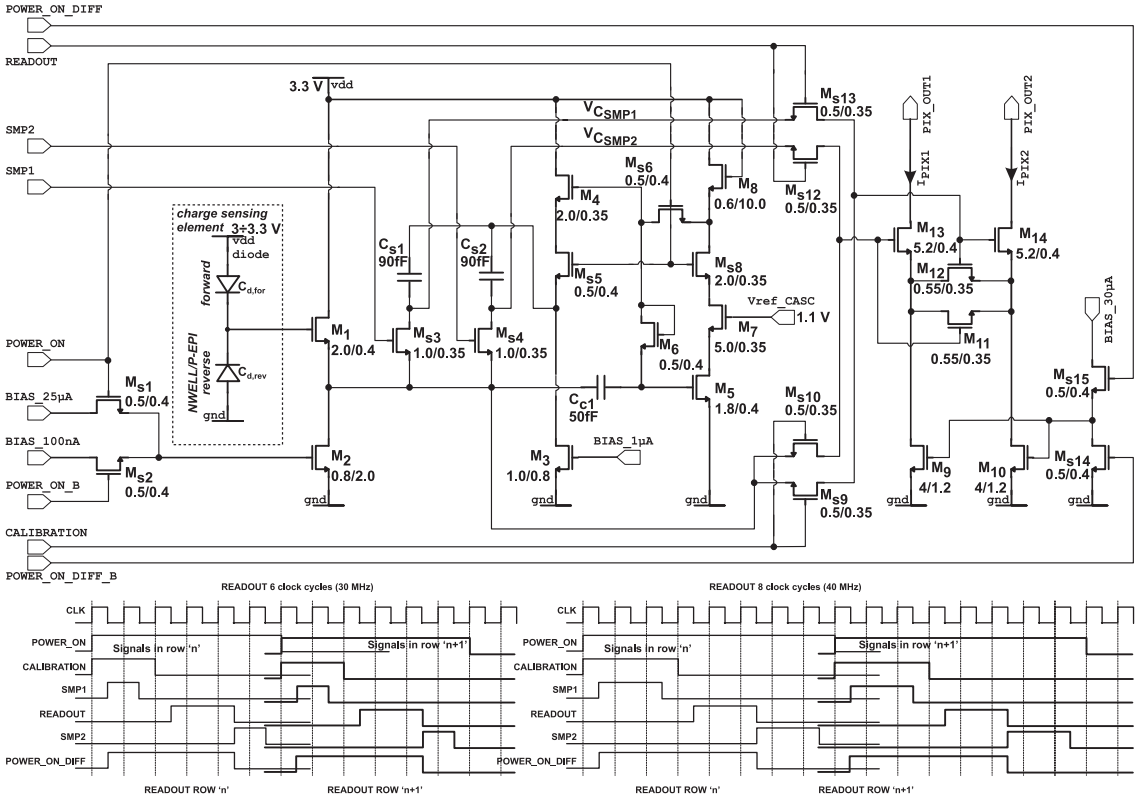

Figure 7-8: Schematic and timing diagrams of the proposed pixel design combining on-pixel amplification with double sampling operation and direct difference signal output.

The on-pixel amplifier comprises three stages. The first stage is a source follower, built with transistors M_1 and M_2, which goal is to buffer the charge sensitive element. Its small input capacitance allows to maximise the charge-to-voltage conversion gain achieved on the first stage. The current of the source follower is switched, by means of transistors M_{s1} and M_{s2}, between two nominal values of 100 nA and 25 μA. The low current value is applied during the charge integration and the high current is turned on when the pixel is addressed to be read out. It is apparent, that the noise of the whole system is dominated by the first stage,

i.e. the source follower. The relatively high bias current applied during the read-out phase is chosen maximising a small signal transconductance of the source follower transistor, which is advantageous for optimisation of the noise performance. On the other hand, the non-zero bias current applied during the charge integration phase is applied to limit voltage variations on the charge-collecting element. These voltage variations are observed as a result of the switched operation between the "on" and "off" states of the pixel. The strongest variations are present for signal integration intervals, which have non-uniform lengths during the detector operation or at the restart of the detector operation after some idle time. The origin of these voltage level variations is linked to the source follower transistor. When the bias current of the source follower transistor is forced to 0 A, the source potential approaches the voltage level of positive power supply. This derive time constant is very long. The change of the source potential affects the transistor gate potential. The reaction of the two-diode system is to return the voltage level to the state in which the currents of both diodes are balanced. As a result, turning on the bias current affects the gate potential of the source follower transistor via a capacitive coupling. The difference between two consecutive "on" states can be interpreted as the presence of a signal in the detector.

The second amplification stage is a common source cascode amplifier AC-coupled by means of a small 50 fF capacitor C_{c1} to the source follower stage. The cascode amplifier features two storage capacitors of 90 fF implemented to be switched on alternatively in the feedback loop. The cascode amplifier is built with the transistor M_5 in the common source configuration, the cascode transistor M_7 and the load transistor M_8 connected in a diode configuration. The bias current of the amplifier is stabilised by a DC feedback loop realised with the transistor M_6 in the diode configuration. The transistor M_6 is operated in deep sub-threshold region at the gate-source voltage close to zero. The channel of the transistor M_8 conveys only a small value current compensating leakage currents discharging the gate of the transistor M_5. This configuration results in a very high equivalent resistance present in the feedback path of the amplifier, which, combined with the parasitic input capacitance of the amplifier, forms a low-pass filter. The very low value of its cut-off frequency assures not altered transfer of the amplified physical signals. The two storage capacitances are alternatively connected in the feedback loop by transistor switches M_{s3} and M_{s4}. They are driven by an additional source follower stage built with transistors M_4 and M_3. The bias

current of the cascode amplifier is set close to 10 μA and the bias current of the second source follower is set to 1 μA. Transistors M_{s5}, M_{s6} and M_{s8}, used as switches, turn on the bias currents in the amplifier during the read-out phase.

The third amplification stage is a linearised, source degenerated differential pair, built with transistors M_{11}, M_{12}, M_{13}, M_{14}. This stage is used as an output transconductance element [116]. The bias current of the differential pair is set to 30 μA, and is provided by two current source transistors M_9 and M_{10}. Other transistor switches M_{s15} and M_{s14} are used to cut off the bias current during the charge integration phase.

In the array structure, the current mode outputs of all pixels in one column are ganged together, and only one pixel addressed for readout, is allowed to drive the lines. In order to allow efficient signal discrimination at the column end, the pixel output signals require correction for offsets present due to dispersion of the transistor parameters in the differential stage. Thus, the calibration operation is foreseen to be performed at the beginning of each read-out phase. For this purpose, the transistor switches M_{s9} and M_{s10} are used to short inputs of the differential pair during the calibration phase. As a result of the calibration phase, the offset currents of the differential pair can be sampled and the corresponding voltage information stored on the external to pixel capacitances. Then, the sampled values of offsets are used for correction of the signal currents read out when transistor switches M_{s12} and M_{s13} get closed and which are proportional to the difference of charges stored on capacitors C_{s1} and C_{s2}. The storage capacitors placed in the amplifier feedback loop play an additional role of Miller capacitances limiting the frequency bandwidth of the source follower. The source follower stage yields the major contribution to the total noise. Thus, the reduced bandwidth of this stage is important, allowing improving noise performance of the whole system.

The pixel circuitry is designed to run in a cyclic continuous mode, where the amplified samples are stored on two capacitances implemented on the pixel. Data taken during the most recent phase is used as the reference level for the next phase. Two nominal modes of pixel operation are foreseen. The timing diagrams of both modes are shown in the bottom side of Figure 7-8. The first mode uses the read-out clock frequency of 30 MHz, while in the second mode the pixel is clocked at 40 MHz. The whole read-out operation occurs in 6 and 8 clock cycles in the first and second operation mode, respectively. For the period when a pixel

is addressed, four consecutive operations are performed. The pixel is switched on applying positive pulses on the *POWER_ON* and *POWER_ON_DIFF* lines. Correspondingly the front source follower with the cascode amplifier and the differential pair are switched on. Initially, a calibrating signal is activated, which shorts the differential input of the on-pixel transconductance stage, allowing correction for offsets in the whole analogue channel. This is achieved by activating the *CALIBRATION* line. The first signal sampling operation occurs simultaneously with the calibration phase. To store the signal sample on one of the feedback capacitances, the positive pulse is sent on the *SMP1* line. The most recent signal is stored on one of the capacitances, while the other one contains the reference level taken in the previous read-out phase. The third operation is the signal read-out phase, during which the current proportional to the difference between the most recent signal and the reference level is available. The read-out phase occurs during the high state on the *READOUT* line. The whole cycle is finished by sampling a new reference value for the next read-out operation activating the *SMP2* signal.

The simulated response of the pixel amplifier to the charge signal injected onto the charge collecting diode, measured as a voltage difference on two storage capacitors, shows the gain of ~0.10 mV/e^- and ~0.09 mV/e^- for schematic only and post-layout simulation, respectively. The corresponding results of the pixel response simulation to the charge signal of 1000 e^- are shown in Figure 7-9. The transconductance value of the differential stage is close to 100 μS, and its output current response was optimised to be linear within the extended range of the differential input voltage of up to more than ±400 mV.

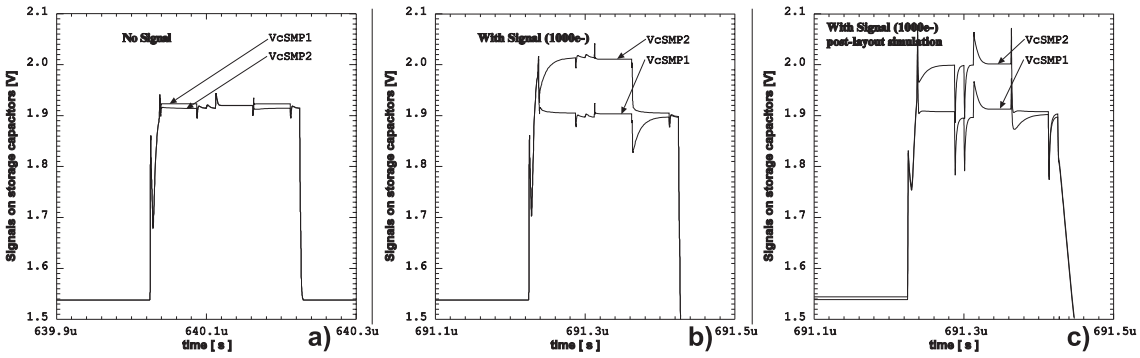

Figure 7-9: Simulated response of the pixel amplifier, measured as a voltage on two store capacitors, (a) in the case of absence of any charge deposited, (b) and for signal equal 1000 e^- schematic only, and (c) post-layout simulation.

The resulting dependence of the differential output current signal as a function of the input signal magnitude is shown in Figure 7-10. A post-layout simulation obtained both curves shown in this figure with all parasitic capacitances extracted.

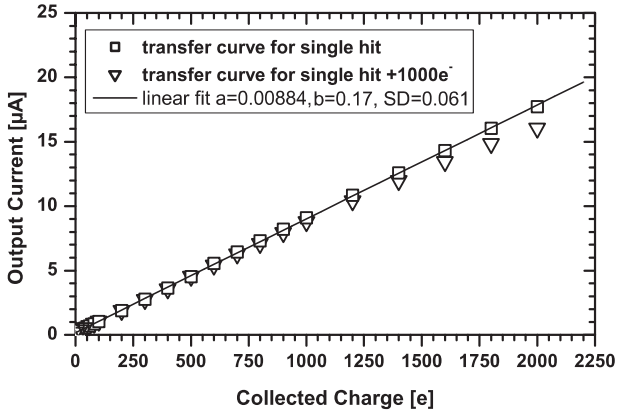

Figure 7-10: Simulated current gain of pixel as a function of the acquired charge.

The first curve, which is marked with squares, illustrates the case of a single hit signals occurring in a detector with amplitudes amounting up to 2000 e^-. The slope of this curve determines the charge-to-current conversion gain of the pixel, which is close to 90 $\mu A/e^-$ after back annotation of parasitic capacitances. This value exhibits approximately 10% loss in the conversion gain with respect to the value found in simulations on schematics neglecting parasitic capacitances. The second curve, marked with triangles, slightly deviates from the linear dependence. It is plotted for a signal, which is superimposed onto another signal of 1000 e^- already deposited in the detector one readout cycle before. The simulation was obtained for a serial read-out of pixels with the time interval between two consecutive readout operations equal to 25.43 µs. This value is characteristic of the MIMOSA VI chip design, where 128 pixels arranged in a single column are read out at the main clock frequency of 30 MHz using the 6-clock cycle readout-timing mode. The considered read-out scheme is related to the periodical switching on of the bias currents in a pixel.

The small signal response of the on pixel amplifier designed for the MIMOSA VI prototype is shown in Figure 7-11. The signal gain measured on the load transistor M_8 is referenced to the input voltage source replacing the charge sensitive element. The transfer function shows the band-pass filter characteristics. The low band cut-off frequency depends on a signal magnitude. It shifts towards higher frequencies for higher signal magnitudes. This

effect results from the increased transconductance of the transistor M_6 with increasing signal amplitudes. In the case of the output signal amplitudes surpassing a few hundred millivolts or in the case of accumulation of many physics hits characterised by the total collected charge of more then 3000 e^- in a short time interval, this effect gives rise to clamping of output signal level.

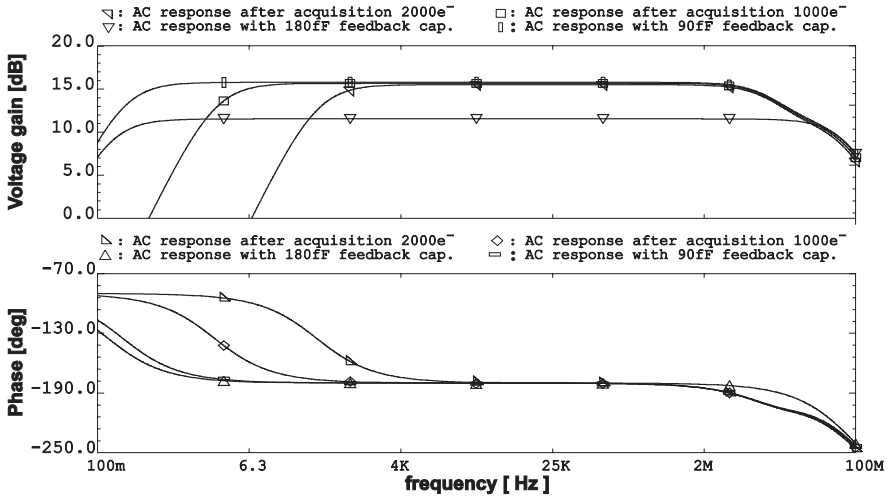

Figure 7-11: Small signal response of the on pixel amplifier.

Column lines ganging current outputs of numerous pixels exhibit a significant parasitic capacitive load. In the case of the MIMOSA VI prototype, featuring 3.6 mm long metal lines and 128 pixels wired to one column, the value of one line parasitic capacitance was estimated to be close to 3 pF. In devices planned for future submissions, the expected capacitive load will be higher, because of larger dimensions of the pixel array. In the MIMOSA VI design, a simple column termination circuitry, as shown in Figure 7-12, was used for analogue signal outputs. A decrease of the resistive load of both column lines, allowing to adapt the column level circuitry to 40 MHz read-out clock frequency, was achieved a cascode stage. The column level circuitry was built with transistors M_{c1} and M_{c2} used as cascode loads, transistors M_{b1} and M_{b2} in the branch supplying an additional current of about 50 μA biasing the cascode transistors and a current mirror with a multiplication factor of 10. The total current conveyed by transistors M_{l1} and M_{l2} amounts in absence of any physical signal to 80 μA and transistors M_{m1} and M_{m2} supply the amplified current directly to the output pads of the chip.

The expected dispersion of pixel-to-pixel charge-to-current conversion gain values was estimated performing Monte Carlo simulations, basing on the process mismatch parameters.

Unfortunately, there was no information for this kind of analyses for the process used of the MIMOSA VI design.

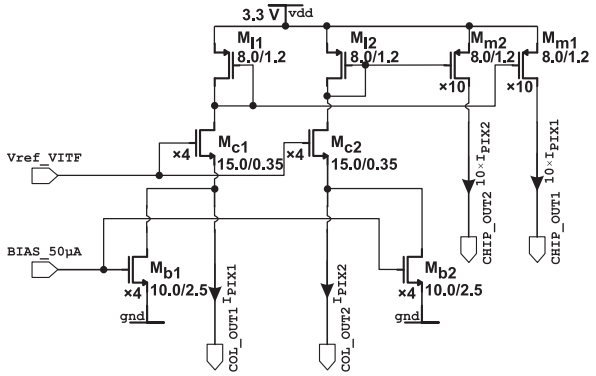

Figure 7-12: Column cascode termination circuitry.

As a consequence, Monte Carlo simulations were done for the design transferred into another 0.35-µm process, namely the AMS process, of which mismatch parameters were known. Assuming a perfect cancellation of offsets for the differential pair during the calibration phase, a pixel gain dispersion of less than 10% was calculated. The results obtained in the Monte Carlo simulation are shown in Figure 7-13.

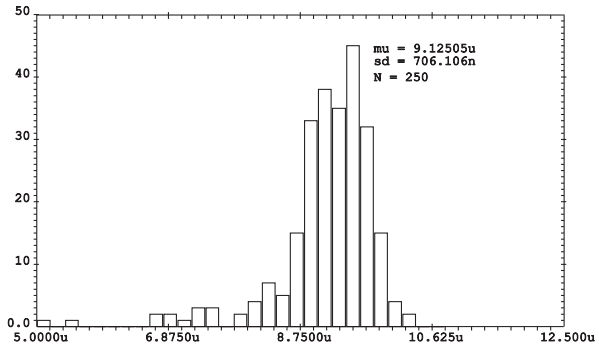

Figure 7-13: Dispersion of the pixel current gain as a result of mismatch variation obtained in the Monte Carlo simulation.

Figure 7-14 shows the final version of the pixel layout implemented on the MIMOSA VI chip. The layout of the pixel implementing on-pixel signal amplification and double sampling operation has been realised in a 0.35 µm CMOS process featuring two polysilicon layers used for design of linear capacitances and five metal layers for interconnections.

The layout of the pixel fits the square area of $28 \times 28\ \mu m^2$ where two versions of the charge collecting diodes of different dimensions, i.e. $4.0 \times 3.7\ \mu m^2$ and $5.0 \times 4.7\ \mu m^2$ have

been implemented. The post-layout simulations showed, that special care was needed to provide immunity of the design to parasitic coupling of the digital control signals to the analogue amplification chain. Because of the floating configuration, the gate of the transistor M_6 was particularly sensitive to the digital signal feedthrough. The use of complementary signals for driving the pixel and carefully chosen distribution of signal lines over the pixel area allowed to suppress the interferences to the tolerable level of only a small fraction of the physical signal expected.

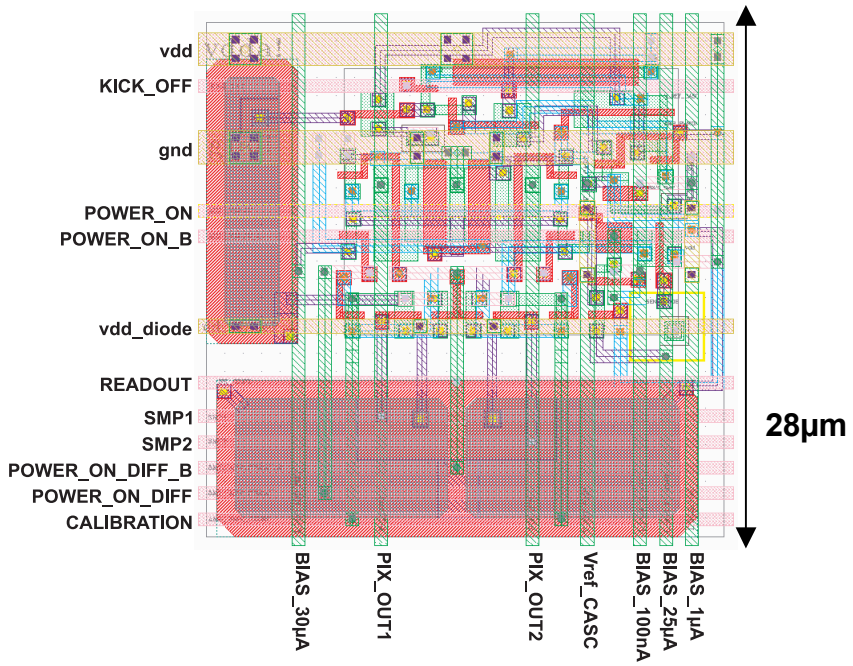

Figure 7-14: Layout of the pixel designed to perform on-pixel signal amplification and double sampling operation.

7.3.2 Current Mode Pixel Concept – PhotoFET

7.3.2.1 Current Mode Charge Sensitive Device

A current mode pixel design is proposed as an alternative approach to increase the sensitivity of the pixel response to the charge generated inside the active detector volume. The novel charge-sensitive element is called photoFET and its design is based on the use of a standard PMOS transistor located in a floating n-well region implanted in the p-type substrate. The concept presented in this chapter resembles pixel architecture, whose successful operation has already been achieved in applications for visible light detection [117, 118, 119]. The structure, to which the reference is made, exhibits much higher

photosensitivity than photodiodes for visible light detection. The generated by incident photons e-h pairs at the neutral substrate and at the n-well/substrate junction affect the threshold voltage of the PMOS transistor, and hence, modulate its channel current. Modulation of the transistor current is synonymous with signal amplification resulting in conversion of the light generated charge to current. A PMOS transistor used for light detection is met to be operated in two different configurations. The first solution assumes a constant voltage bias on the front polysilicon gate of the device and reset operation performed before each light measurement. The reset of the n-well, in which the photosensitive PMOS transistor is implanted, to the positive power supply voltage level delimits beginning of charge integration interval. The photo-generated charge collected by the n-well, left floating during the integration phase, affects the well potential and thus changes the threshold voltage of the MOS device. In this way, the drain current modulated from the back-gate is achieved. The bias drain current, thus the operation region of the transistor, is determined by the constant potential applied to the transistor gate. The sensitivity depends on the operating point. Resignation from the periodically performed reset operation of the charge collecting n-well yields the structure, which is sensitive to the transient illumination level. The output current characteristic of the PMOS transistor has been reported as a result of measurements to exhibit logarithmic dependence on the photon flux when operated in strong inversion. While, it becomes nearly linear for the PMOS transistor operated in weak inversion. The extremely high photosensitivity of the element was measured in visible light spectrum to be as large as 1000 A/W, when operated in strong inversion. The device is fitted to deal with low irradiation levels due to its intrinsic transistor amplification. The disadvantage of the current mode structure can be the fact that the speed of the output current response to any light intensity variation depends on the mean value of light intensity. Similarly to the two-diode design described in Chapter 7.3.1, the potential of the n-well is a logarithmic function of a light power. The leakage current of the n-well/p-substrate junction as well as the transient current emptying the n-well from charge carriers originating from light conversion are conveyed by the p^+/n-well diode. This diode is associated with the PMOS transistor source diffusion and in absence of any light signal it carries only the leakage current. The p^+/n-well diode is biased slightly in forward direction and represents although non-linear but of very high value resistance. Thus, at low

illumination levels, charge integration with a long decay time constant occurs and the diode connection assures continuous reverse bias of the n-well/p-substrate junction. The second option of a PMOS transistor based visible light detector opts for further increase of the device sensitivity. In this solution, the n-well potential modulated by light illumination is fed back to the front gate through the well-to-gate connection. This connection results in an extra current amplification beyond that of a normal PMOS transistor driven from the substrate. The n-well to polysilicon gate connection is left floating during normal operation. As the n-well is connected to the polysilicon gate, both the n-well and the gate are self-biased by the forward voltage generated by optical illumination. The gate voltage follows the potential change of the n-well. The sensitivity of the device is largely determined by the optically induced voltage between the gate to n-well combination and the substrate. The gate voltage of the PMOS device, assuming a linear dependence of the optically generated current on the optical power and the exponential dependence of the current conveyed by the p^+/n-well source diode on the voltage across the junction, exhibits the ideal slope for the n-well potential versus light intensity of 60 mV/decade of light power. A disadvantage of this solution is a nearly zero value of the device transconductances both from the polysilicon gate and the substrate under dark conditions and for low illumination levels. In the darkness, the n-well potential is determined by the n-well/substrate leakage current, resulting in the PMOS transistor drain current in the order of picoamperes.

7.3.2.2 Design of the Pixel with PhotoFET Element and Double Sampling Operation for Charged Particles Detection

Negligibly low transconductance of the detector element exploiting a PMOS transistor exploiting a floating configuration of the n-well and the transistor gate connected together excludes its use for charged particle detection and tracking. For this application, a high transconductance value is required for the whole operation region of the device. Particularly, high transconductance is required for the device operated in darkness waiting for any physical signal occurrence. This is a typical operation regime of the vertex detector. A new highly responsive sensor element is proposed here. It provides a built-in signal amplification capability, resulting in charge-to-current conversion, and self reverse biasing of the charge-collecting element. Conceptual design of this novel charge sensitive element, called

photoFET, is shown in Figure 7-15. The design is fully compatible with a standard CMOS process. The sensor is unique in that the n-well is connected to the polysilicon gate of a PMOS transistor passing via a source follower transistor. The source follower transistor intrudes some voltage shift between the n-well and polysilicon gate potentials, which is necessary to bias the PMOS transistor in the region of high transconductance value. The n-well to the source follower transistor connection is left floating during operation. The photoFET device may resemble the DEPFET device discussed in Chapter 3.3.4. The resemblance is only partial. Although both devices realise conversion of the collected charge into current, the details of operation are distinct. The photoFET device uses thin undepleted substrate as an active detector volume and standard CMOS process for fabrication. Contrary to the DEPFET device, where the charge is stored on the internal gate requiring periodical clearing via the clear gate, the photoFET device collect the charge directly in the transistor substrate and continuous clearing of the collected charge is achieved by a diode polarised weakly in forward direction.

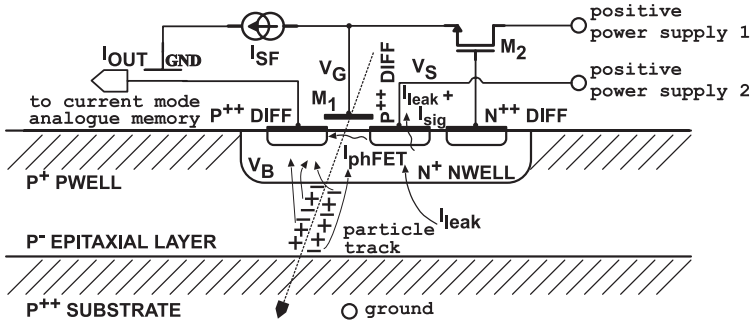

Figure 7-15: Conceptual design of pixel structure with built-in amplification and continuous reverse bias of the diode for charge collection.

Schematic diagram of the complete pixel design, exploiting novel charge sensitive element implemented in a 0.35 μm CMOS process, is shown in Figure 7-16. This figure gives an idea on a complete current mode pixel design as well as on timing diagrams proposed to operate the array of active cells built based on the photoFET element with the PMOS transistor M_1 and the source follower transistor M_2. The operation in low or strong inversion regions of the photoFET device depends on the bias current of the source follower transistor. In order to keep the PMOS transistor drain current at room temperature in the single microampere range, the source follower transistor bias current is set to the value in the

order of a few tens of nanoamperes. The low value of the bias current is required from practical point to limit the power consumption. The design of a charge sensitive element introduces some additional parasitic capacitances due to the presence of metal interconnection lines and the gate-to-drain capacitance of the source follower. These capacitances are not present in the design featuring constant voltage bias of the PMOS transistor gate. However, the gain due to the front gate transconductance, which has a value typically 3 to 5 times higher than the transconductance from the bulk for modern processes, fully compensates losses in the charge-to-voltage conversion gain due to the increased conversion capacitance.

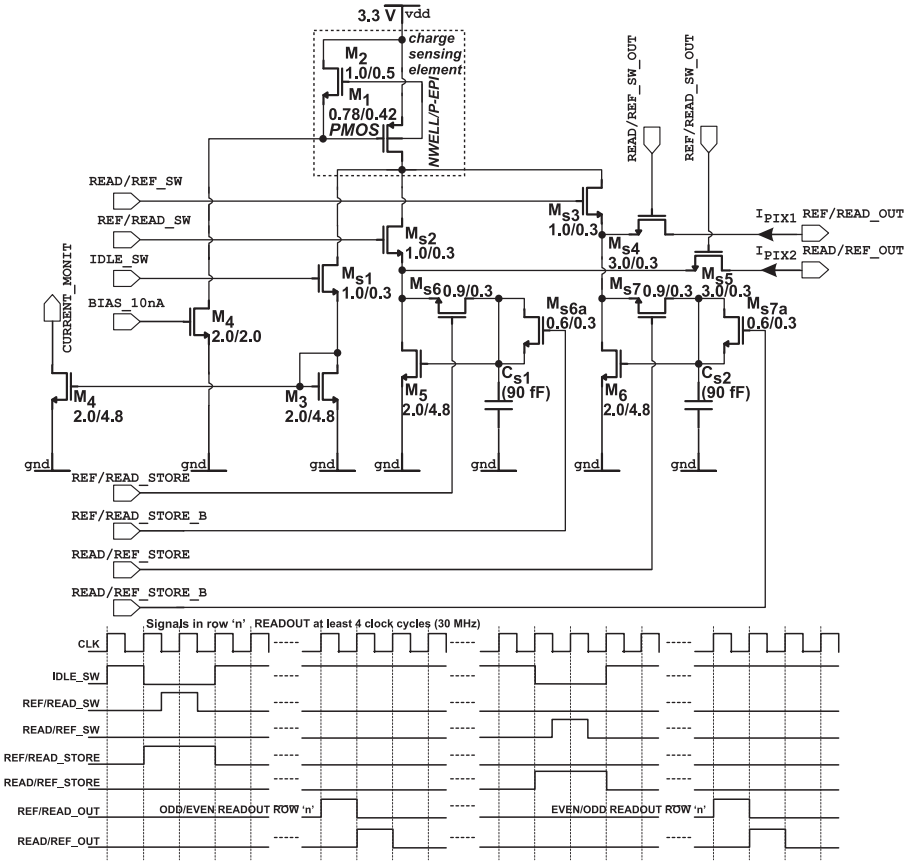

Figure 7-16: Schematic and timing diagrams of the current mode pixel design proposed, photoFET.

A single read-out operation, according to the timing diagram presented in Figure 7-16, occurs in at least four clock cycles of a 30 MHz read-out clock. The *IDLE_SW* signal is set active switching on the M_{s1} transistor switch throughout all the time except only the time when the pairs *REF/READ_STORE* – *REF/READ_SW* and *READ/REF_STORE* –

READ/REF_SW are activated. When the *IDLE_SW* signal is active the photoFET drain current is available as mirrored by the current mirror built with transistors M_3 and M_4. Anticipating good noise performance of the photoFET device, the ganged *CURRENT_MONIT* outputs of some number of pixels can be used to provide a kind of trigger signalling the presence of a hit. This would allow to restrict the read-out to small size sub-arrays of pixels in the whole detector only. The pixel from these sub-arrays can be accessed taking advantage of selective addressing access to pixels capability and the accurate signal from a single pixel can be sent to the data acquisition system. The *REF/READ_SW* and *READ/REF_SW* signals are used to switch the current from the photoFET element, using transistor switches M_{s2} and M_{s3}, to one of two analogue memory cells implemented in pixel in Figure 7-16. The first cell, built with transistors M_5, M_{s6} and M_{s6a} and the capacitor C_{s1}, and the second one, built with transistors M_6, M_{s7} and M_{s7a} and the capacitor C_{s2}, store current signal samples, which become alternatively the reference and the current signal values for double sampling of signals performed outside the pixel. The current samples are frozen in the memory activating correspondingly the *REF/READ_STORE READ/REF_STORE* signals. The samples of currents are available for further off-pixel processing, e.g. consisting in their subtraction and amplification with conversion on corresponding voltage signals, after activating the *READ/REF_SW_OUT* and *REF/READ_SW_OUT* signals. The last two signals are used effectively for pixel addressing.

The test structure, consisting of the photoFET charge sensitive element, the system of current mode analogue signal memories and a simple transimpedance amplifier performing subtraction of two current samples, has been implemented on the periphery of the MIMOSA IV chip. Tests of electrical and X-ray detection performances of the pixel with the novel charge sensitive element are under way. The results obtained recently are much better than those obtained formerly with a PMOS transistor featuring constant voltage bias of its source-to-gate voltage implemented as a test structure in the MIMOSA II chip[*]. The sample of recent results obtained with soft X-ray photons from ^{55}Fe is shown in Figure 7-17. The plot shows the output of the current monitor port of the photoFET device and the output of the transimpedance amplifier performing on-line double sampling and conversion to

[*] Results, because of their marginality, are not reported in this work. In this case, the mean SNR for X-ray photons from a ^{55}Fe source was measured to be in the order of 10.

voltage of signals sampled on current mode memories on the pixel as a function of time. Each point in this figure represents data taken after integration time equal to one millisecond. Preliminary results obtained with the photoFET device provide the estimation of an output current response sensitivity about 330 pA/1e$^-$ at constant bias current of about 5 μA and a noise level, measured as a sampled signal variance in the frequency bandwidth from 1 kHz to 25 MHz, at the level between 1.4 nA to 2.2 nA. These values are in good agreement with prior SPICE simulation and analytic calculations.

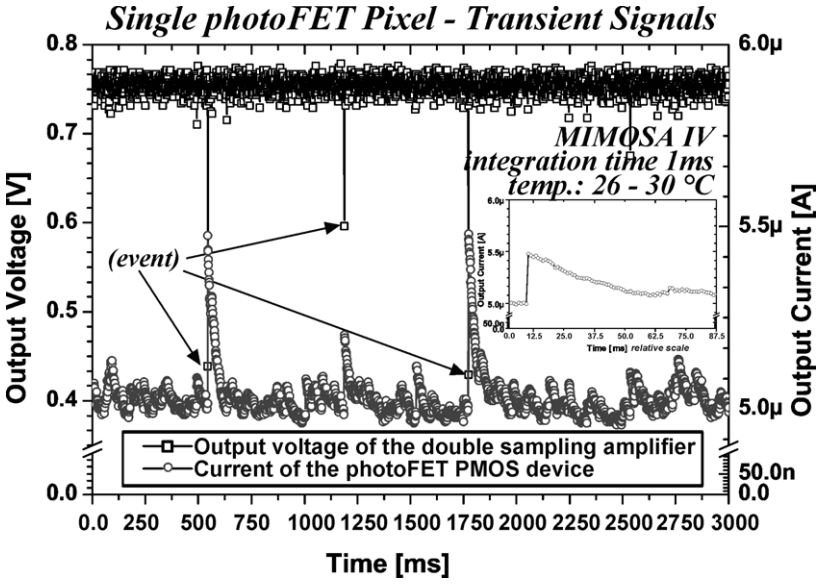

Figure 7-17: Preliminary results obtained in tests of a photoFET device with 5.9 keV X-ray photons.

In future designs of the photoFET element, the power supply for the source follower and PMOS transistors can be separated. The higher power supply value for the source follower transistor with respect to the PMOS transistor allows to increase the source follower transistor bias current, while the bias current of the PMOS device can remain unchanged conserving power consumption. A higher value of the source follower bias current is advantageous in view of its noise performance. In the same time, attention is needed to reduce the bulk effect on the source follower in order to allow easy control of the operation region for the PMOS transistor. In a standard approach, relatively high gate-to-source voltage of the source follower transistor due to the strong bulk effect force the PMOS to operate in strong inversion. Strong inversion operation of the PMOS transistor is undesirable, because of higher power consumption and non-linear characteristic of the transfer function.

Reduction of bulk effect for the source follower transistor can be achieved using fabrication processes featuring so-called "triple well" option.

Operation of the photoFET element is based on transistor bulk effect i.e. the modulation of the transistor threshold voltage V_{TH} by the substrate voltage due to the accumulated charge

$$V_{TH}\left(V_{BS}\right) = 2\phi_{F_n} - \frac{qN_D L_D}{C_{ox}}\sqrt{2\frac{q\left|2\phi_{F_n} - V_{BS}\right|}{kT}}, \tag{7-1}$$

where V_{BS} is the bulk to source voltage of the PMOS transistor, N_D is the n-well doping concentration and L_D is the Debeye length defined as

$$L_D = \sqrt{\frac{\varepsilon_0 \varepsilon_{Si} kT}{q^2 N_D}}, \tag{7-2}$$

where $\varepsilon_{Si} = 11.9$ is the dielectric constant of silicon, and ϕ_{F_n} is the Fermi potential in the n-well transistor substrate given by

$$\phi_{F_n} = -\frac{kT}{q}\ln\frac{N_D}{n_i}, \tag{7-3}$$

The front-side transconductance g_m for an input signal on the gate the PMOS transistor in strong inversion is defined as

$$g_m = \frac{dI_{DS}}{dV_{GS}} = \sqrt{2\frac{W}{L}\mu C_{ox} I_{DS}}, \tag{7-4}$$

and the backside transconductance, g_{mb}, or drain current sensitivity for an input signal on the n-well is given by

$$g_{mb} = \frac{dI_{DS}}{dV_{SUB}} = -g_m\frac{dV_{th}}{dV_{SUB}} = \frac{qN_D L_D}{\sqrt{C_{ox}}}\sqrt{\frac{q}{kT\left|2\phi_{Fn} - V_{sub}\right|}\cdot\frac{W}{L}\mu I_{DS}}. \tag{7-5}$$

For the photoFET device with the n-well coupled to the polysilicon gate, both transcoductances give their contribution to the PMOS transistor drain current. Even in the absence of any physical signal, the bias current of the device is determined by the non zero gate-to-source voltage of the source follower transistor. This voltage introduces shift between the n-well potential, which is the substrate for the PMOS transistor and its gate.

The SPICE simulation of the photoFET device as well as the operation of other structures, having non-standard functionalities or operation regions, are out of scope of

device models included in SPICE simulator, and therefore are very difficult. Often it is necessary to combine elements, which are well modelled in SPICE with additional circuitry rendering particular physical behaviour, for example charge accumulation in the n-well. The results obtained in such simulations are likely to suffer from limited modelling accuracy. Thus, precise simulations carried out using software tools for semiconductor process and device simulation are necessary. The optimisation of the photoFET structure is planned to be carried out using the ISE-TCAD package, which is one of these tools.

7.4 Perspectives for the Fabrication Processes

The detailed tests of the prototypes already fabricated, in four different CMOS processes, have shown that the epitaxial layer thickness should be in excess of several micrometers, the optimum thickness being around 10 μm in the case of a 20 μm pixel pitch. The doping level translating in the highest achievable resistivity of 10 Ωcm or more is required. These values account for the fraction of the total charge spreading among neighbouring pixels for optimal tracking resolution and the satisfactory track separation. However, further investigations are needed before one can conclude on the optimum balance between the epitaxial layer thickness, the pixel pitch and doping level as functions of the relevant signal parameters, e.g. collection efficiency, charge collection speed, read-out speed and spatial resolution. Moreover, the role and the control of the substrate in the signal generation, which may yield a significant contribution to the total signal depending on temperature and doping level, needs to be better understood and potentially explored.

The choice of the fabrication processes used for the next steps of the development of MAPS detectors requires continuous survey of CMOS processes evolution. The use of a standard process requires to follow technology trends and to subordinate the design to the technology supplier and the technology market. This effort is remunerated in a high fabrication yield and a good prototyping price. Besides the performances of the technology for detector designs, special care for the long-term accessibility of the process is important. Deep sub-micrometer technologies with minimal feature sizes around 0.25 μm could meet now this requirement, while offering great integration capability and radiation resistance, which has already been ascertained with standard CMOS electronics, designed for other high energy physics experiments. High integration capability for the integration of various

functionalities directly on the sensor substrate is required.

Driven by the increasingly growing market of consumer imaging application for visible light, semiconductor foundries offer CMOS processes with a feature size of 0.25 μm and below, which are specialised and optimised for image sensor fabrication. These processes are characterised by low leakage currents of photodiodes below 0.1 nA/cm^2. A thick epitaxial layer is also provided since it is required to be in the order of 8 μm - 10 μm for efficient absorption of red light. Processes, optimised for CMOS image sensor, feature full analogue option for mixed mode applications including precise linear capacitors and resistances. The number of metal layers amounts up to 3 - 5, which is a bit less than for a standard modern mixed mode processes featuring up to nine metal layers. The limited number of available metal layers results from the reduction of material on top of light sensitive elements for improving the detection of blue light. However, this is not a concern and compact routing is still possible. The presence on the market of processes optimised for image sensor fabrication is very optimistic for MAPS detector technology, however their easy accessibility is questioned for a niche domain of MAPS detectors for applications in particle and nuclear physics experiments. Profits from this small-scale production are negligible for a foundry, when compared to large volume commercial production of digital cameras.

The modern deep sub-micrometer CMOS processes are developed as so called triple-well processes. In this case, a moderately doped p-type substrate is used as a base material, and PMOS transistors are implanted traditionally in an n-well. However, fabrication of NMOS transistors requires implantation of two wells. As a first step, a deep n-well is created, in which, as a second step, a thinner p-well is implanted. The p-well becomes a substrate for an NMOS transistor. Such fabrication technology is advantageous allowing to increase the immunity of circuits to interferences, cross talks and latch-ups without a requirement for thin epitaxial layer. Also stacked in series NMOS transistors does not suffer from the bulk effect, known from increasing their threshold voltages when devices are fabricated in a standard process. Thus, for triple well processes low power supply voltage of 1.25 V can be exploited in a more efficient way. Positive experience gained with the MIMOSA IV chip, which was fabricated on the wafer without an epitaxial layer, shows that the MAPS technology should also be compatible with the triple-well technology option.

Chapter 8

SUMMMARY AND CONCLUSIONS

8.1 Work Summary

The initial proposition of MAPS detectors, based on the use of a standard CMOS process for construction of a high precision and high efficiency systems for charged particle detection has been fully demonstrated. A new monolithic pixel detector has been developed and extensively tested. Pixel detectors of high granularity, integrated with the read-out electronics circuitry on the same substrate allow to precisely determining the particle position under the high density of impinging particles environment. The ability of monolithic CMOS sensors to provide charged particle tracking has been measured on a series of MIMOSA chip prototypes. The tests demonstrate that devices exploiting this detection technique work efficiently and provides excellent tracking quality. The estimated experimental performances, which are well reproduced by the simulations, show that the sensors provide excellent conditions for pattern recognition and for determining MIPs impact positions with an accuracy satisfying the requests of the most demanding vertex detector designs of the upcoming generation. The main requirements for a vertex detector at a future collider experiment are already fulfilled with the sensor prototypes tested. Some other requirements are still to be met, but the new research axes have been traced out based on the current status of the experience acquired. The MAPS detectors are also attractive candidates for application in other domains requiring charged particle imaging. The operation of the MAPS detectors can be carried out at room temperature and only standard power supplies for integrated circuits are required to bias the whole device. The sequential nature of the read-out was determined in the prototypes fabricated by the logic circuitry only. Random access would require only modification of the logic, and not of the analogue part of the circuitry.

In order to integrate a complete detection system on the same chip, many critical data processing specific components must be developed in a deep sub-micrometer process, using dedicated design rules to assure required radiation hardness. This is a particular issue and will be the subject of on-going work. This future work includes investigating possibilities of

integrating various read-out functions directly on the sensor and thinning down the substrate to the limits set by its mechanical properties.

The conveyed research studies, covered by this work includes realisation of the following stages:

1. The essential parameters of the fabrication process affecting performances of a detector were identified, and the choice of processes applicable to detector fabrication was done bearing in mind results of this review. The key element is the use of a moderately doped medium, most favourably at the resistivity level of 10 Ωcm or more, as an active detector volume underneath the read-out electronics. The active detector volume can be an epitaxial layer of usually 2 μm – 15 μm thicknesses grown on a highly doped silicon base or non-epitaxial, so-called high resistive wafers for manufacturing of integrated circuits can with similar success be used. The optimum thickness of the active layer has been identified to be around 10 μm in case of a 20 μm pixel pitch. However, the freedom in the choice for the optimum device thickness is limited, since most of the time this is specified by the manufacturer as fixed value for a particular CMOS process. A small size, ensuing small charge-to-voltage conversion capacitance, n-well/p-epi diode paving and access to the active detector volume was used for collecting the charge generated by the impinging particle. This solution allows 100% fill factor, as required in tracking applications. The striking feature in MAPS operation is the charge collection achieved through thermal diffusion, since the active detector volume has no electric field. The charge carriers diffuse and continuously get reflected between the potential barriers formed in the interfaces of the epitaxial layer and the substrate as well as of the epitaxial layer and the p-well until they get collected at the diode. Improvements in the collection element consisting, firstly in continuous reverse bias of the diode replacing vexatious periodic pixel resetting, and secondly in structures allowing obtaining signal gain directly in the charge-sensing element have been proposed.
2. In the MAPS detectors, the total amount of charge, which can be collected at the electrodes, is proportional to the thickness of the active volume. Increasing the thickness of the detector active volume, although advantageous for the amplitude of the signal, increases collection time and cluster size, owing to the increased side diffusion of the mobile excess charges. It is not easy to calculate in an analytical way the optimum

geometrical configuration of the detector conditioned by the properties of the fabrication process foreseen for the detector fabrication. Thus, the detailed device simulation based on the ISE-TCAD package, exploiting the developed MAPS detector model, was carried out. Parameters governing efficient charge collection have been addressed. The thickness of the epitaxial layer, the pixel size, the number of the collecting diodes per single pixel cell and their size were considered the physical parameters having the most decisive effect on the charge collection for doping profiles characteristic for a given fabrication process. These quantities were used as parameters in simulations. The read-out circuitry was designed in a way allowing to test efficiently the prototypes fabricated. Emphasis has been laid on noise performance and read-out speed optimisation. New pixel designs and read-out concepts have been proposed to match signal discrimination and data sparsification to be implemented on the chip in future. The new ideas were implemented for their validation on the most recent MIMOSA prototype submitted already for fabrication.

3. Four small-scale prototype detectors have been designed and fabricated in 0.6 μm, 0.35 μm and 0.25 μm processes with epitaxial layer and in a 0.35 μm non-epitaxial layer process. The prototypes feature pixel arrays of different design. Among other things, some of the matrices were designed using radiation tolerant layout rules and design options with more than one charge collecting diode per pixel and staggered pixel layouts were tested. One large wafer size MIMOSA device has been designed and fabricated in a 6" wafer process. The related tests after thinning down the device to 120 μm are under way.

4. The charge collection time of MIMOSA I was measured with infrared laser shots and compared to the result of three-dimensional simulations based on the ISE-TCAD package.

5. The performances of four small scale prototypes were measured in necessary laboratory electrical bench tests and exposing them to visible light using light emitting diodes LED and soft X-ray radiation from a radioactive source of 55Fe and high energy particle beams from the PS and SPS accelerators at CERN. A detailed analysis of the data collected was performed, where most of the noise was eliminated by the Correlated Double Sampling processing and the result summary has been provided. Simulations and

results obtained throughout the design process were compared with the experimental data, yielding high degree of agreement and confirming correctness of the adopted assumptions, e.g. noise optimisation procedure, properties of charge collection, etc. The immunity of the new detection technique to damaging radiation was tested exposing the chips to different kinds of radiation i.e. protons, X-ray photons and neutrons. This pixel device, in which the signal spreads over different cells, is not the optimal device to do spectroscopy. The substantial fraction of tests, including the calibration of the charge-to-voltage gain and verification of the detector performance degradation after irradiation, was done using soft X-ray radiation as an excitation source showing good SNR behaviour and uniformity of the tested arrays.

6. The performances of the MAPS detectors were verified to be retained under the influence of strong magnetic field of different orientation with respect to the detector surface.

7. The first research phase consisted primarily of demonstrating that the sensor technology was adequate for charged particle detection. In parallel to the optimisation of the intrinsic detector performances an important effort is needed to find an efficient solution for the read-out architecture and on-chip data processing. The work oriented on the development of the read-out method matching the requirements for data processing and data transfer in the real vertex detector has been initiated in the design of the MIMOSA V chip already mentioned and particularly in the MIMOSA VI chip. The latter is a device featuring first design attempt for on-pixel signal amplification and double sampling pixel operation. The chip design exploits column parallel signal processing, integrating discriminators at the end of each column.

8.2 Conclusions

A major advantage of MAPS, as it has already been in the case of CCDs, is that the High Energy Physics benefits from the multi-disciplinary user base of these devices. Technological progress, made by industrial manufacturers is driven mainly by the consumer-end oriented community for visible light imaging applications. High Energy Physics provides a rather small and irregular market for developing and industrial maintaining dedicated to one specialised application of fabrication processes. This purely scientific market is insufficient to sustain a

major industrial R&D programme and cannot guarantee stability of the process. In contrast to that, the use of a standard, well-established industrial process, assures high fabrication yield. The design of the MAPS detectors for charged particle detection and tracking is based largely on the major progress having been made over 10 last years by the CMOS APS designers and manufacturers for commercial customers.

The beam tests demonstrate that this detection technique works very efficiently and provides excellent tracking performances. Thanks to the technology used for their fabrication, monolithic CMOS devices are likely to provide a cost-effective solution for high precision tracking systems, combining advantages of CCDs and Hybrid Pixel Detectors. When applied to charged particle tracking, a MAPS detector concentrate actually the positive features of the CCDs and exhibit several additional advantages, some of them covering areas where hybrid pixels are better of than CCDs. Radiation tolerance for instance benefits from sub-micrometer technology and from the conversion of the signal charge inside the pixel where it was created. The read-out speed, on the other hand, benefits from the possibility to integrate much functionality on the sensor substrate. They consume little power as the circuitry in each pixel is only active during the read-out, as it was the case in the first small size MIMOSA prototypes, and as there is no clock signal driving large capacitances.

The measured tracking performance of minimum ionising particles includes very high spatial resolution of 1.5 μm and the detection efficiency close to 100%, resulting from a high SNR of more than 30. The time it takes to collect the charge is about 100 ns. Hence, the absence of any drift field does not entail a fundamental limitation in the response time of the detector at least for experiments not requiring more precise time stamping. The radiation hardness test results are also satisfactory, offering a security margin at least one order of magnitude above the radiation doses predicted at future linear colliders, which are for example in the case of the TESLA experiment: 100 krad for the ionising dose and a neutron fluence of 5×10^9 integrated over five years of operation.

In short, a new pixel detector integrating on the same substrate the detector element and the read-out electronics was developed, and gave excellent results. However, still considerable amount of work needs to be done before operating this structure in any future experiment. The established intrinsic performances of the sensor technology are likely to be subject of improvement since the technology potential is still far from being explored. Such

investigations aim at, among others, reducing the electronic noise, improving the charge collection efficiency, exploring various manufacturing processes, finding the optimal operation conditions in terms of temperature, SNR, read-out speed and research towards the optimum detector read-out architecture incorporating fast and efficient data sparsification.

APPENDIX

A. Noise in Classical Front-End Electronics for a Hybrid Pixel Detector

For the read-out system shown in Figure 3-10, assuming a MOS transistor as an input device, the noise power spectral density at the preamplifier output can be expressed as

$$S_{\substack{v_{out}^2 \\ PREAMP}}(f) = \left|\frac{C_d + C_i + C_f}{C_f}\right|^2 S_{v_i^2}(f) + \left|\frac{1}{2\pi j f C_f}\right|^2 \left(S_{i_d^2}(f) + S_{i_{lc}^2}(f)\right), \tag{A-1}$$

where the power spectral densities of noise sources at the preamplifier input, $S_{v_i^2}(f)$, $S_{i_d^2}(f)$ and $S_{i_{lc}^2}(f)$ are given by the relevant equations

$$\begin{aligned} S_{v_i^2}(f) &= \frac{K_a}{C_{ox}^2 W_{Min} L_{Min}} \frac{1}{f} + \frac{4kTn\gamma_{Min}}{g_{m,Min}}, \\ S_{i_d^2}(f) &= 2qI_{leak}, \\ S_{i_{lc}^2}(f) &= \frac{K_a\left(I_{leak} + I_{bias,Mlc}\right)}{C_{ox} L_{Mlc}^2 f} + \frac{4kTn\gamma_{Mlc}}{g_{m\,Mlc}}, \end{aligned} \tag{A-2}$$

where K_a is a constant depending on the nature of the gate oxide, C_{ox} is a gate oxide capacitance per unit area, $W_{M<...>}$ and $L_{M<...>}$ are the dimensions of the specified transistor, k is Boltzmann constant, T is the absolute temperature, n is a parameter relevant to the sub-threshold characteristic, $\gamma_{M<...>}$ is a coefficient depending on the operating region of the given transistor (weak, moderate or strong inversion) and $I_{bias,Mlc}$ is the constant bias current in the leakage current compensation branch. The noise power spectrum at the output is weighted by the transfer function of the shaper. The total integrated r.m.s. noise is thus obtained by integration over infinite frequency range

$$v_{\substack{out \\ SHAPER}}^2[rms] = \int_0^\infty \left| S_{\substack{v_{out}^2 \\ PREAMP}}(f) \right| \left| H_{SHAPER}(2\pi j f) \right|^2 df, \tag{A-3}$$

where $H_{SHAPER}(2\pi j f)$ is the transfer function of the shaper. Referring to a semi-gaussian

shaper containing n_{sh} integrators ($CR-RC^{n_{sh}}$*), the maximum amplitude of the output signal due to the charge, Q, generated in the detector is given by

$$V_{\substack{out \\ SHAPER}}\Big|_{max} = \frac{q A^{n_{sh}} n_{sh}^{n_{sh}}}{C_f n_{sh}! e^{n_{sh}}}, \tag{A-4}$$

where q is the magnitude of the electron charge and A is the DC gain of each integrator in the shaper. The number of integrators, n_{sh}, is referred to as the order of the pulse shaper [120]. The three ENC components $ENC_{f_0}^2$, $ENC_{1/f}^2$, ENC_d^2, which are due to the channel thermal noise of the input transistor, its flicker noise, and the detector leakage current, respectively, are given by

$$\begin{aligned} ENC_{f_0}^2 &= \frac{4kTn\gamma_{Min}}{g_{mMin}} A_{f_0} \frac{\left(C_d + C_i\right)^2}{\tau_s} \\ ENC_{1/f}^2 &= \frac{K_a}{C_{ox}^2 W_{Min} L_{Min}} A_{1/f} \left(C_d + C_i\right)^2, \\ ENC_d^2 &= A_d I_{leak} \tau_s \end{aligned} \tag{A-5}$$

where A_{f_0}, $A_{1/f}$ and A_d are noise coefficients depending on the actual order of the pulse shaper and they represent the amplifier white noise, flicker noise and the detector shot noise contributions, respectively. The term τ_s is the peaking time equal to the product of the integrators time constant and the pulse shaper order.

The remaining ENC component resulting from operation of the leakage compensation circuit can be calculated by

$$\begin{aligned} ENC_{lc}^2 &= 4kTn\gamma_{Mlc} g_{m,Mlc} A_{f_0}^{lc} \tau_s + \frac{K_a g_{m,Mlc}^2}{C_{ox}^2 W_{Mlc} L_{Mlc}} A_{1/f}^{lc} \tau_s^2 I_O, \\ g_{m,Mlc} &\propto \left(I_{leak} + I_{bias,Mlc}\right) \end{aligned}, \tag{A-6}$$

where $A_{f_0}^{lc}$ and $A_{1/f}^{lc}$ are, as previously, noise coefficients for the amplifier white and flicker noise and I_O is given by the following integral

---

* The CR-RC filter of the n_{sh}-th order is constructed by one RC differentiator and n_{sh} integrators, which in general case are realised as active circuits.

$$I_O = \int_{\frac{1}{2\pi\tau_{lc}}}^{\infty} \left(\frac{1}{\left(1+\left(2\pi f\tau_s\right)^2\right)^2} \frac{1}{f} \right) df \,. \tag{A-7}$$

The lower limit of the integral is determined by the low cut-off frequency, $1/\left(2\pi\tau_{lc}\right)$, of the preamplifier due to the presence of the feedback loop of the leakage current compensation circuit and is equal to its time constant. Usually for the fast applications, the flicker noise component in (A-1) is small and the thermal noise component dominates. Assuming weak inversion operation of the transistor, Mlc, in the leakage compensation circuit, the ENC due to the current compensation circuit can be given using the simply equation,

$$ENC_{lc}^2 = A_d \left(I_{leak} + I_{bias,Mlc} \right) \tau_s \,. \tag{A-8}$$

For higher values of leakage current, which satisfy the relation between the constant bias current $I_{leak} >> I_{bias,Mlc}$, moving the transistor, Mlc, in to strong inversion operation the ENC_{lcs}^2 becomes minor when compared with ENC_d^2.

The total ENC for the CMOS front-end readout system is given by

$$ENC = ENC_{f_0}^2 + ENC_{1/f}^2 + ENC_d^2 + ENC_{lc}^2 \,. \tag{A-9}$$

To minimise the total ENC the amplifier must be designed to minimise the noise contribution within the amplifier with respect the input stage and to have as large as possible transconductance of the input stage $g_{m\,Min}$, and the input capacitance satisfying the optimal noise matching condition [120].

B. Generation of Charge Carriers in MAPS Simulations

Alpha Particle Model

The charge generation function, implemented for alpha particles in DESSIS-ISE is given by formula (B-10) with conditions (B-11) and (B-12). The default parameters of this function had to be modified in order to obtain the generation rate-emulating minimum ionising particles. The set of coefficients used for the *alpha-particle* model adapted in this way, is listed in Table B-1.

$$G(x,v,w,t)=\begin{cases}\dfrac{a}{s\sqrt{2\pi}}e^{-\frac{1}{2}\left(\frac{t-t_m}{s}\right)^2}e^{-\frac{1}{2}\left(\frac{v^2+w^2}{w_t^2}\right)}\left[c_1e^{\alpha x}+c_2e^{-\frac{1}{2}\left(\frac{x-\alpha_1}{\alpha_2}\right)^2}\right] & \text{if} \quad x<\alpha_1+\alpha_3\\ 0 & \text{if} \quad x\geq\alpha_1+\alpha_3\end{cases}, \tag{B-10}$$

where x is the distance along the particle track, v and w are the two orthogonal co-ordinates transverse to the trajectory. The parameter t_m is the time of the generation peak, w_t defines the radial distribution of the liberated charge along the particle track and α_1 is the maximum of the Bragg peak, which together with the parameter c_1 is expressed by

$$\alpha_1=a_0+a_1E_n+a_2E_n^2 \quad \text{and} \quad c_1=e^{\alpha(\alpha_1[10\,\text{MeV}]-\alpha_1[E_n])}. \tag{B-11}$$

where scaling coefficients a_0, a_1, a_2 are obtained from a fit to the experimental data. The scaling factor a in formula (B-10) is determined in following integration

$$\int_0^\infty\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}G(x,v,w,t)\,dt\,dw\,dv\,dx=\frac{E_n}{W}, \tag{B-12}$$

where W is the energy needed in average to create an e-h pair, and E_n is the assumed energy of the particle. In the simulation, E_n =2.88 × 10^6 eV, t=0 s, and the impact position was parameterised.

Table B-1 Coefficients for the charge generation rate according to the *alpha-particle* model to emulate charge liberated due to passage of a minimum ionising particle.

Model parameters									
w_t	c_2	α	a_0	a_1	a_2	α_2	α_3	W	s
0.75 × 10^{-4} [cm]	0 [-]	1.0 × 10^{-15} [cm^{-1}]	1.0 [cm]	0 [cm/eV]	0 [cm/eV^2]	1 [cm]	0 [cm]	3.6 [eV]	0.1 × 10^{-9} [s]

Figure B-1 shows charge generation rates of a constant value 76 e-h pairs per micrometer of the distance traversed by the impinging particle and a gaussian distribution characterised by a sigma of 0.75 μm defined tranversaly to the particle track. The charge generation rate has been obtained according to the *alpha-particle* model adapted to simulate minimum ionising particles.

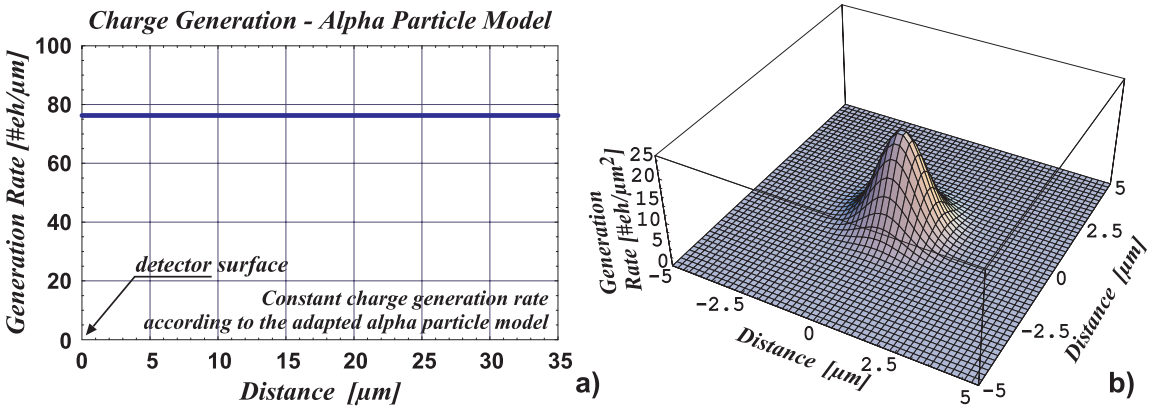

Figure B-1: (a) Charge generation rate as a function of the distance traversed by the impinging particle, (b) gaussian distribution of charge generation rate transversally to the particle track.

Heavy Ion Model

This model was used to describe a point-like excess charge generation due to a single X-ray photon interaction in the simulated detector.

A particle traversing a device looses energy creating a trail of electron-hole pairs. The generation rate in the *heavy-ion* model is computed by

$$G(x,w,t)=\begin{cases} LET(x)R(w,x)T(t) & \text{if} \quad x < x_{max} \\ 0 & \text{if} \quad x \geq x_{max} \end{cases}, \tag{B-13}$$

where x is a distance along the particle track, w is a radial co-ordinate perpendicular to the track and $LET(x)$*, $R(w,x)$ and $T(t)$ are the general functions defining the energy loss rate along the particle track, the initial distribution of the generated carriers as a function of the distance from the track and the time dependence of charge production, respectively. These functions are given by the following formulas:

* The function named LET is used to stand for the Linear Energy Transfer.

$$\begin{cases} \mathrm{LET}(x) = a_1 + a_2 x + a_3 e^{a_4 x} + k_n \left[c_1 (c_2 + c_3 x)^{c_4} + \mathrm{Lf}(x) \right] \\ \\ T(t) = \dfrac{2e^{-\left(\frac{t-t_m}{s}\right)^2}}{s\sqrt{\pi}\left(1 - \mathrm{erf}\left(\frac{t_m}{s}\right)\right)} \quad \text{and} \quad R(w, x) = e^{-\left(\frac{w}{w_t(x)}\right)^2} \end{cases} \text{, where} \tag{B-14}$$

$$k_n = \begin{cases} \dfrac{k}{\pi w_t^2(x)} & \text{if case 3D and } \mathrm{LET}(x) \text{ unit } [\mathrm{pC}/\mu\mathrm{m}] \\ \dfrac{k}{10^{-6}[\mathrm{m}]\, w_t(x)\sqrt{\pi}} & \text{if case 2D and } \mathrm{LET}(x) \text{ unit } [\mathrm{pC}/\mu\mathrm{m}] \end{cases} . \tag{B-15}$$

The charge generation rates can be expressed for the simulation input either in [pairs/cm^3] or preferably in [pC/μm] and can be parameterised along the traversed path. The quantity $\mathrm{Lf}(x)$ is subject to specify in the command file, which is processed by the DESSIS-ISE. It has a form of a list of parameters, where each element specifies ionisation level at the given point on the particle trajectory. The charge generation rate between each pair of points results from interpolation from two neighbouring values. The positions along the particle track are supplied as a separate list in the command file. A point-like energy deposition linked to the impact of a single X-ray photon in the active volume can be modelled by the ionisation given by the following form

$$\mathrm{Lf}(x) = \{0,\ \mathrm{let}(x_1),\ \mathrm{let}(x_2),\ 0\}$$

$$\text{where} \quad \mathrm{let}(x_1) = \mathrm{let}(x_2) = \frac{1.6 \times 10^{-19}[\mathrm{C}]}{(x_2 - x_1)[\mu\mathrm{m}]} \ \frac{\text{photon energy}}{\text{energy / eh pair}} \tag{B-16}$$

Each element of the list (B-16) specifies ionisation. All scaling coefficients in expressions (B-15) and (B-16), used to model the charge liberated due to the impact of an X-ray photon, are given in Table B-2.

Table B-2 Coefficients for the charge generation rate according to the *heavy-ion* model to emulate the charge generated due to the impact of an X-ray photon.

Model parameters									
s	a_1	a_2	a_3	a_4	k	c_1	c_2	c_3	c_4
2.0×10^{-12} [s]	0 [cm^{-3}]	0 [cm^{-3}]	0 [cm^{-3}]	0 [μm^{-1}]	1 [-]	0 [cm^{-3} or pCμm^{-1}]	0 [-]	1 [cm^{-1}]	0 [-]

Figure B-2 shows an example of charge generation rate function obtained at a constant radial distribution of the generated charge $w_t(x) = 0.75\,\mu m$ as a function of the distance from the detector surface at which photon conversion occurs. The charge generation rate has been obtained according to the *heavy-ion* model adapted to simulate charge generation due to 5.9 keV X-ray photons conversion.

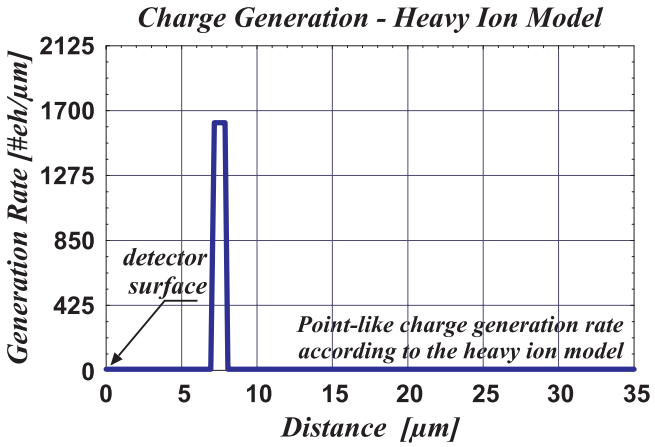

Figure B-2: Charge generation rate as a function of the distance from the detector surface of the example X-ray photon conversion.

C. MIMOSA Chips – Conceptual Design and Pin-outs

The following figures present conceptual views of the MIMOSA prototype chips fabricated in different processes (0.6 μm, 0.35 μm with and without epitaxial layer and 0.25 μm) and details of the layouts of basic cells used in each design. The small arrows in the figures, presenting composition of the chips, indicate directions in which the read-out of pixels in each array is arranged. The read-out is performed in a serial way, where the analogue data is shifted out in a consecutive clock cycles. Numbering of pixels corresponds to the appearing order in the serial analogue data at the chip output. The short description of the main features of arrays of pixels implemented on each chip, including their dimensions expressed in number of pixels and details on particular pixel configuration, is given as well. Furthermore, the figures contain information on squared and staggered layouts of pixels used for particular arrays. In the case of staggered layouts, the figures show the actual arrangement of shifted rows in an array corner where the read-out process starts. The information on the arrangement of the staggered rows is of great importance for the beam test data analysis, allowing easier detector plane positioning and orientation in the reference system of the beam telescope. The signal assignment information, i.e. the pin-out of each chip is also shown in the successive figures. This information is useful for a designer who is about to realize electrical inter-connections to the PCB motherboard, while designing the system based on the MIMOSA chips. The remaining figures show layouts of basic pixel cells implemented in the adequate MIMOSA chip. The pixels were laid out with a uniform pitch in both directions of 20 μm for MIMOSA I, II and IV, and 8 μm for MIMOSA III. The last figure shows the die microphotographs of the fabricated chips.

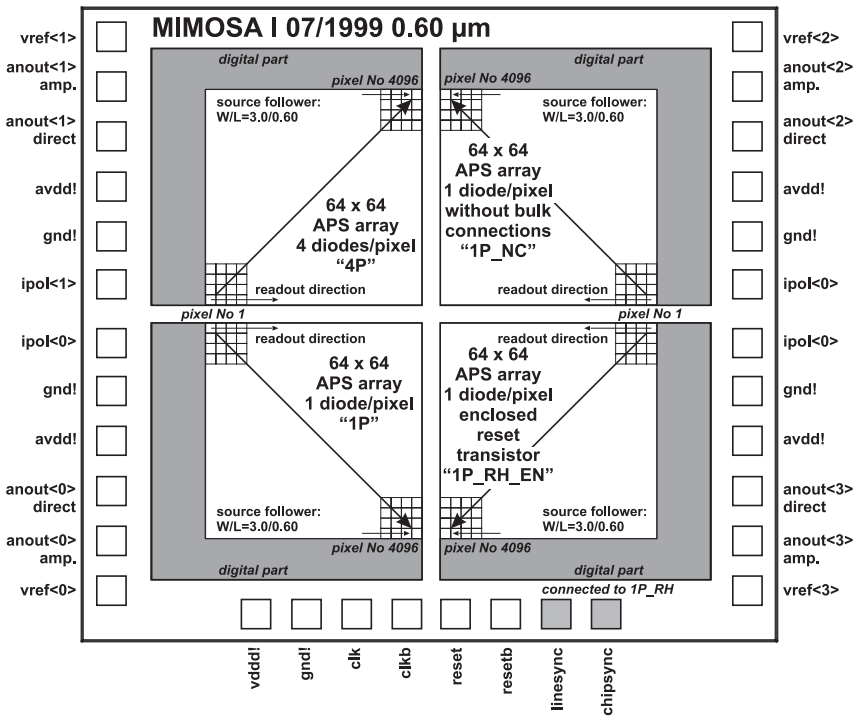

Figure C-3: Simplified structure and pin-out of the MIMOSA I chip (AMS 0.6 µm).

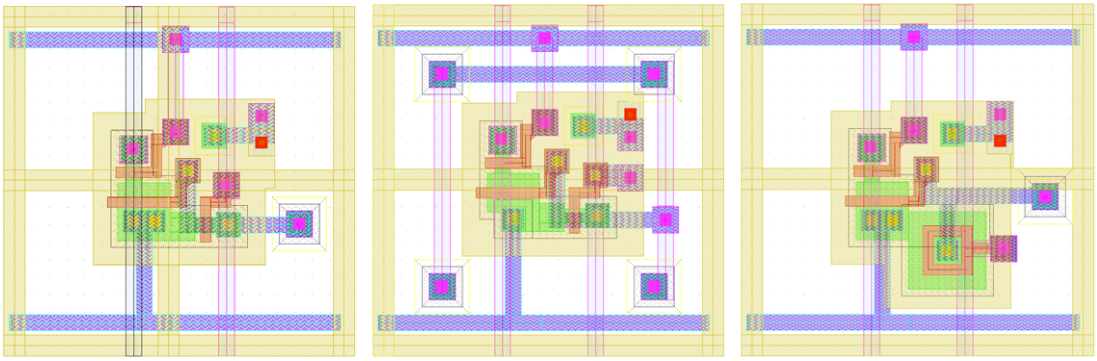

Figure C-4: Example of basic cell layouts in MIMOSA I: (a) single-diode pixel (1P), (b) four-diode pixel (4P), (c) single-diode pixel with enclosed reset transistor (1P_RH_EN). The last metal level (M3) is not shown.

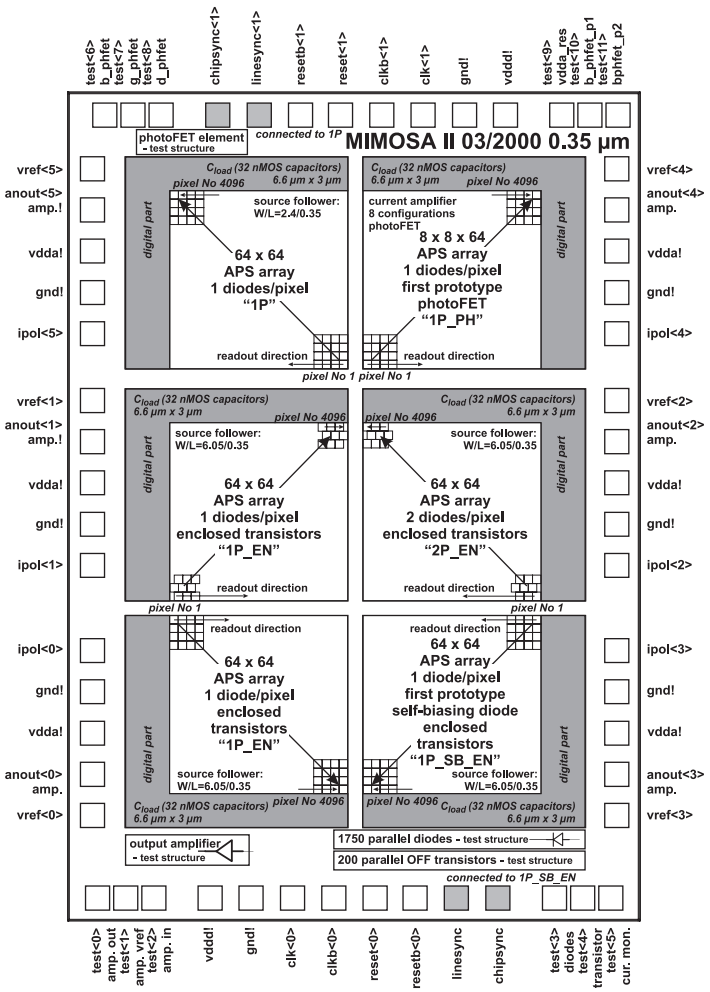

Figure C-5: Simplified structure and pin-out of the MIMOSA II chip (Alcatel Mietec 0.35 µm).

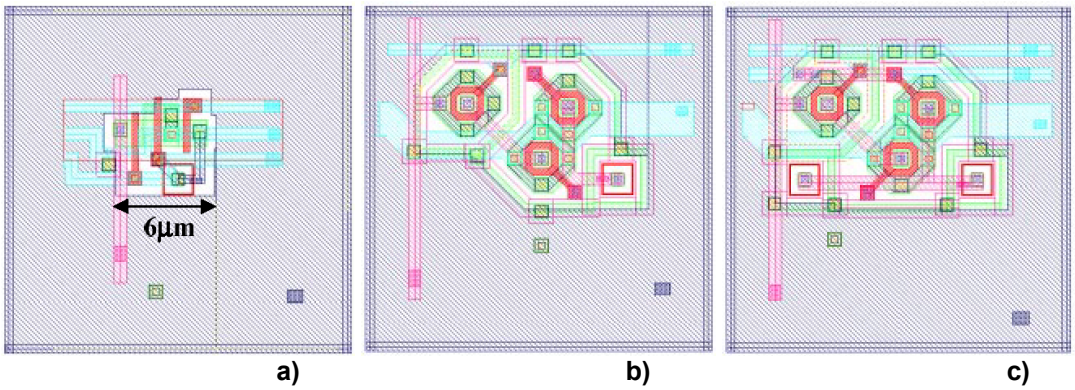

Figure C-6: Example of basic cell layouts in MIMOSA II: (a) single-diode pixel with standard transistor design (1P), (b) single-diode pixel with enclosed transistors (1P_EN), (c) two-diode pixel with enclosed transistors (2P_EN). The last metal levels (M4 and M5) are not shown.

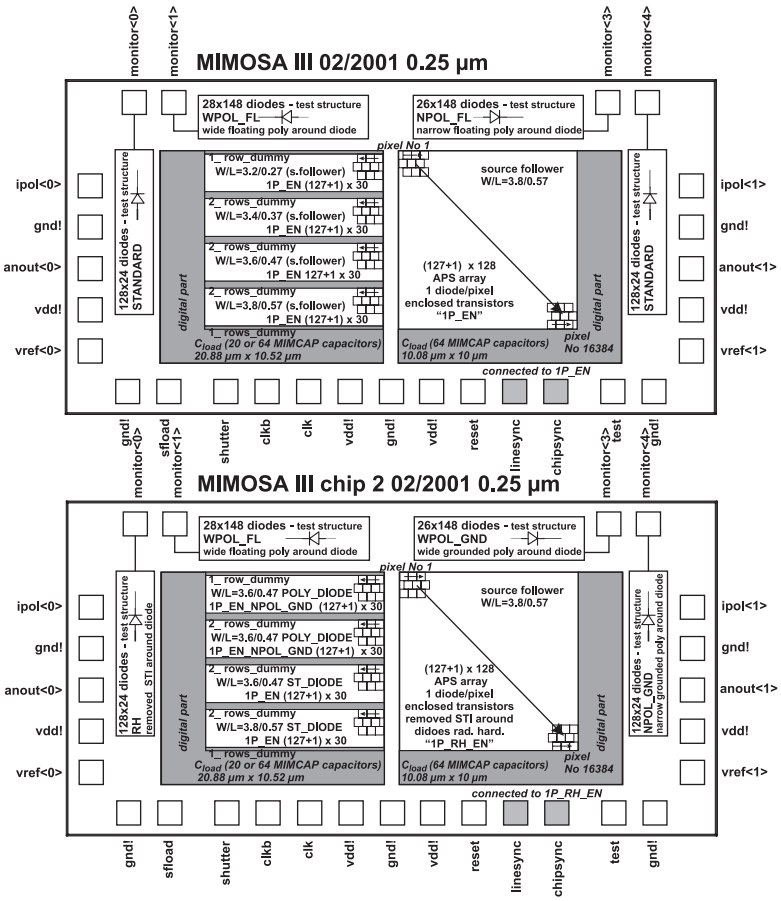

Figure C-7: Simplified structure and pin-out of the MIMOSA III chip (IBM 0.25 µm).

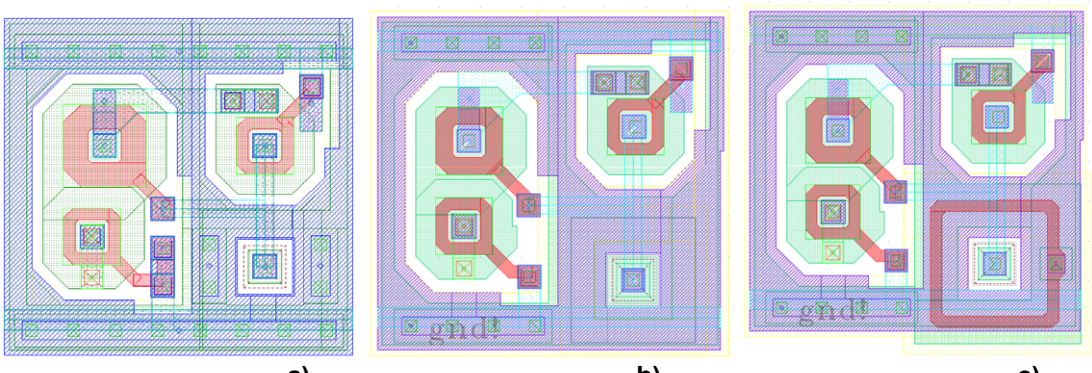

Figure C-8: Example of basic cell layout in MIMOSA III: (a) single-diode pixel with enclosed transistors (1P_EN), (b) single-diode pixel with enclosed transistors and STI region removed in the vicinity of the diode (1P_RH_EN), (c) single-diode pixel with enclosed transistors and polysilicon grounded ring around diode (1P_EN_NPOL_GND). The last metal level (M3) is not shown.

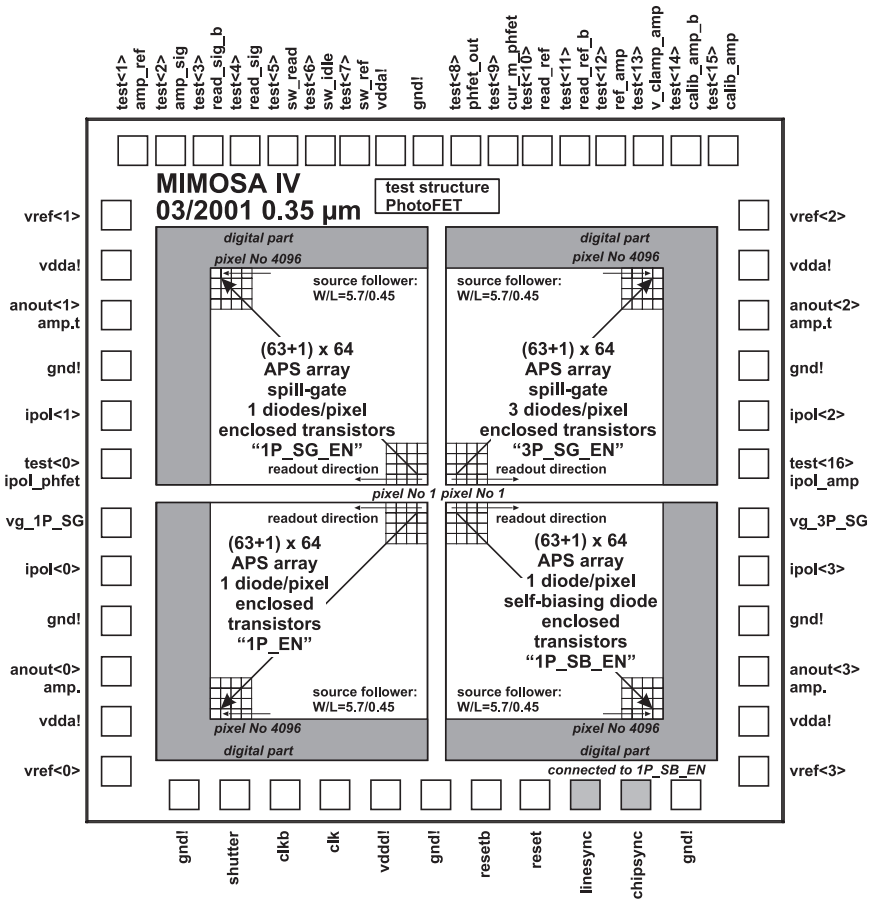

Figure C-9: Simplified structure and pin-out of the MIMOSA IV chip (AMS 0.35 µm).

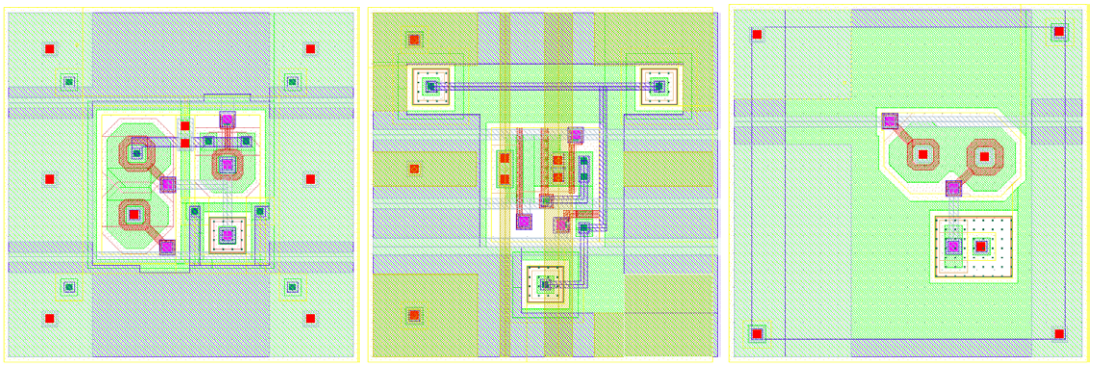

Figure C-10:Example of basic cell layout in MIMOSA IV: (a) single-diode pixel with enclosed transistors (1P_EN), (b) three-diode pixel with enclosed transistors and spill-gate topology (3P_SG_EN), (c) single-diode pixel with enclosed transistors with self-biasing capability of the charge sensing diode (1P_SB_EN). The last metal level (M3) is not shown in (a) and (b).

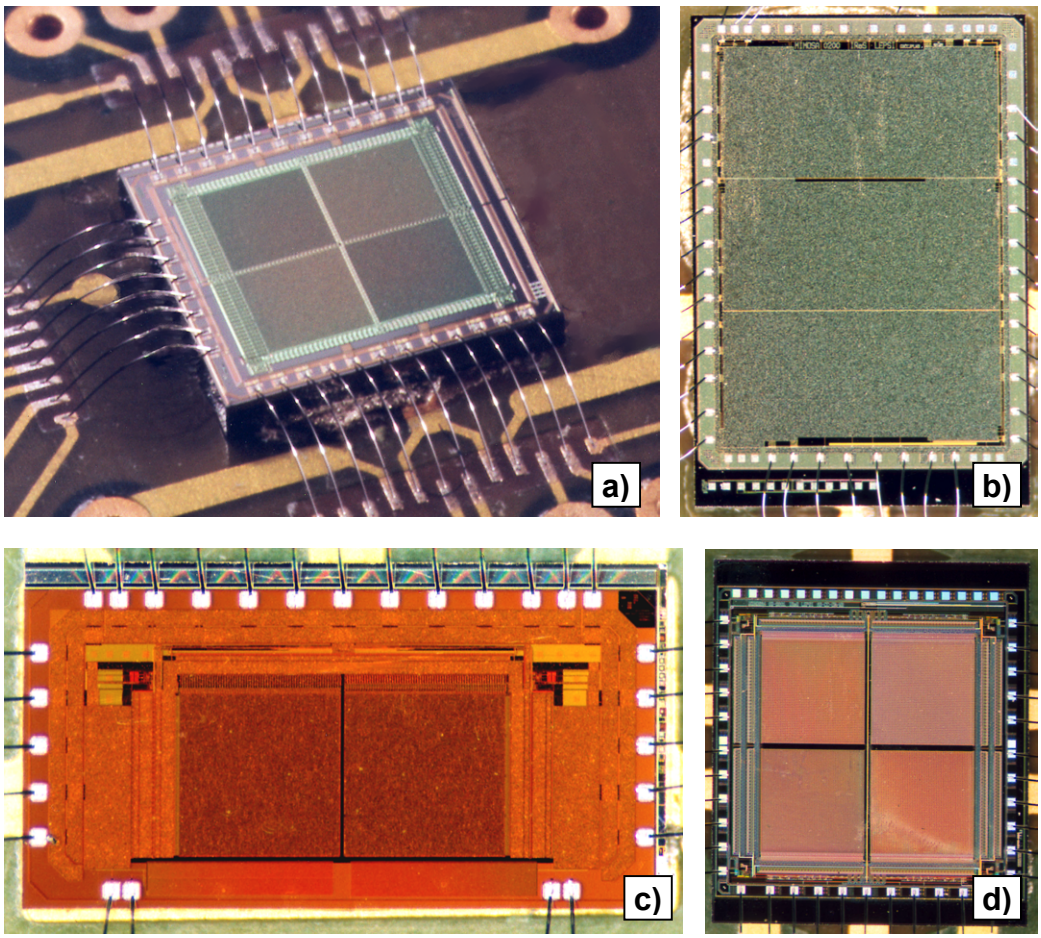

Figure C-11:Die microphotographs of (a) MIMOSA I , (b) MIMOSA II, (c) MIMOSA III and (d) MIMOSA IV.

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Résumé: Les détecteurs de vertex sont importants pour les expériences de la physique des particules, car la connaissance de la saveur présente dans un événement deviendra une question majeure dans le programme de physique auprès du Futur Collisionneur Linéaire. Un capteur monolithique à pixels actifs (MAPS) basé sur une structure originale a été proposé. Le capteur est inséparable de son électronique de lecture, puisque les deux sont intégrés sur la même tranche de silicum basse résistivité qui constitue le substrat classique pour une technologie CMOS. La configuration de base est composée uniquement de trois transistors et d'une diode qui collecte par diffusion thermique la charge. Celle-ci est générée dans la couche épitaxiale mince, non-désertée en dessous du circuit de lecture. Cela permet d'obtenir un détecteur mince, de haute résolution, d'une surface entièrement sensible à la radiation et d'un faible coût de fabrication. Les simulations détaillées ont été effectuées en utilisant le logiciel ISE-TCAD pour étudier le mécanisme de collection de charge. Quatre prototypes ont été fabriqués en technologies CMOS submicroniques pour démontrer la viabilité de cette technique. Le gain des pixels a été calibré par irradiation à l'aide d'une source ^{55}Fe et en appliquant la méthode fondée sur la séquence de Poisson. Les prototypes ont été également exposés aux faisceaux de particules de haute énergie au CERN. D'excellentes performances de détection ont été prouvées. Elles s'expriment par un rapport signal sur bruit supérieur à 30, une résolution spatiale de 1.5 µm et une efficacité de détection proche de 100%. Les tests d'irradiation ont démontré une résistance aux flux de neutrons jusqu'a quelques 10^{12} n/cm^2 et une résistance aux rayonnements ionisants jusqu'a quelques centaines kRad. Des idées futures telles que l'amplification du signal sur le pixel, le double échantillonnage ainsi que la conception d'un pixel en mode courrant ont été également présentées.

Mots-clés: Détecteurs à état solide sensibles à la position, Détecteurs à pixels actifs, Détecteurs monolithiques, CMOS, VLSI, Système sur puce, Trajectographie des particules, Imagerie, Simulation de dispositif, Bas bruit, Tenue aux rayonnements

Abstract: Vertex detectors are of great importance in particle physics experiments, as the knowledge of the event flavour is becoming an issue for the physics programme at Future Linear Colliders. Monolithic Active Pixel Sensors (MAPS) based on a novel detector structure have been proposed. Their fabrication is compatible with a standard CMOS process. The sensor is inseparable from the readout electronics, since both of them are integrated on the same, low-resistivity silicon wafer. The basic pixel configuration comprises only three MOS transistors and a diode collecting the charge through thermal diffusion. The charge is generated in the thin undepleted epitaxial layer underneath the readout electronics. This approach provides, at low cost, a high resolution and thin device with the whole area sensitive to radiation. Device simulations using the ISE-TCAD package have been carried out to study the charge collection mechanism. In order to demonstrate the viability of the technique, four prototype chips have been fabricated using different submicrometer CMOS processes. The pixel gain has been calibrated using a ^{55}Fe source and the Poisson sequence method. The prototypes have been exposed to high-energy particle beams at CERN. The tests proved excellent detection performances expressed in a single-track spatial resolution of 1.5 µm and detection efficiency close to 100%, resulting from a SNR ratio of more than 30. Irradiation tests showed immunity of MAPS to a level of a few times 10^{12} n/cm^2 and a few hundred kRad of ionising radiation. The ideas for future work, including on-pixel signal amplification, double sampling operation and current mode pixel design are present as well.

Key words: Solid-state position sensitive detectors, Pixel detectors, Monolithic Active Pixel Sensors, CMOS, VLSI, System-on-chip, Particle tracking, Imaging, Device simulation, Low noise, Radiation hardness